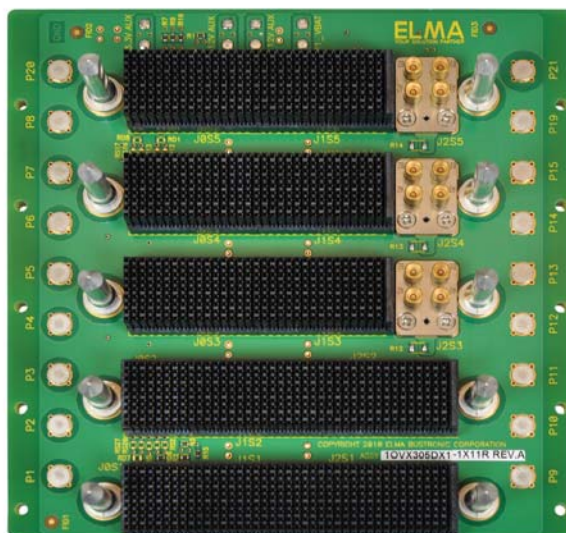


# 3U OpenVPX 5-slot BKP3-DIS05-15.3.2-n Backplane



## Description

The 3U, 5-slot OpenVPX backplane has 3 slots for VITA 67 RF connectors, which are passthrough only. Otherwise, the design incorporates a distributed mesh topology.

## Features

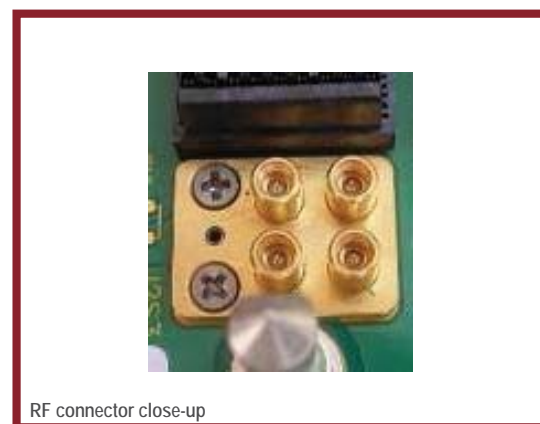
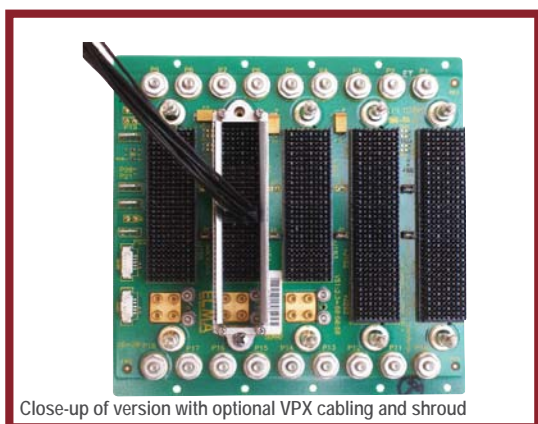
- Compliant to ANSIVITA 65-2010
- Compliant to the latest VITA 46 Specifications
- A 4-cavity RF connector installed in 3 slots of the lower half of the standard J2 connector. This corresponds to rows 9-16 of slots 3, 4 and 5
- High-speed MultiGig connector
- Uses the rugged 3U-160 Eurocard form factor
- Mesh routing topology with all four fat pipes connected across all slots
- Provides built in ESD ground protection in every slot

## Board Specifications

- 14-layer stripline design
- 2 oz. power and ground
- PCB FR-4 or equivalent
- PCB .213" thick

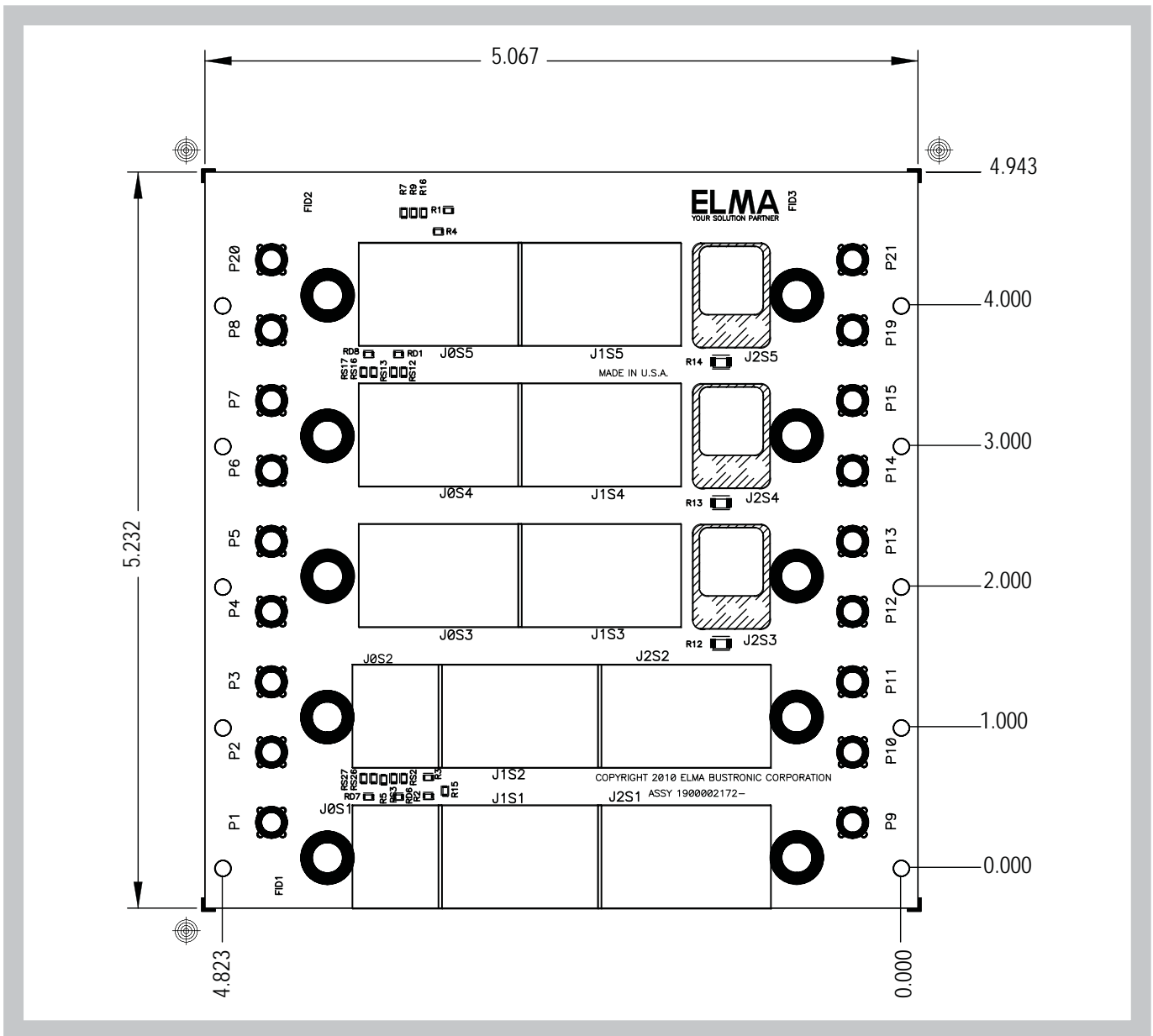
## Mechanical Specifications

- 3U height
- 5 slots
- 1.0" pitch



# 3U OpenVPX 5-slot BKP3-DIS05-15.3.2-n Backplane

## Line Drawing

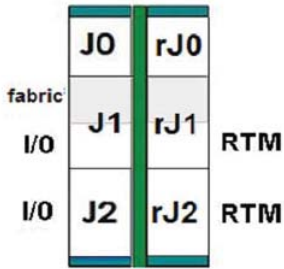


## ORDER INFORMATION

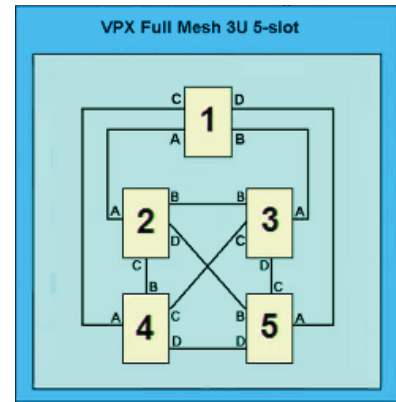
Height	Total Slots	Description	Profile Number	Part Number
3U	5	Mesh with 3 VITA 67 RF connector interfaces	BKP3-DIS05-15.3.2-1	10VX305DX1-1X11R
3U	5	Mesh with 3 VITA 67 RF connector interfaces, no RTM connectors	BKP3-DIS05-15.3.2-1	10VX305DX1-1X10R

# 3U OpenVPX 5-slot BKP3-DIS05-15.3.2-n Backplane

## Connector Positions



## Connectivity Chart



## J0 Signal Assignments

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

## J1 Signal Assignments

Plug-In Module P1	Row G	Row F	Row E		Row D	Row C	Row B		Row A	
			Even	Odd			Even	Odd		
Blplane J1	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a	
Data Plane Port 1	1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
	2	GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
	3	P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
	4	GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
Data Plane Port 2	5	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
	6	GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
	7	Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
	8	GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
Data Plane Port 3	9	UD	GND	GND-J1	DP03-T0-	DP03-T0+	GND	GND-J1	DP03-R0-	DP03-R0+
	10	GND	DP03-T1-	DP03-T1+	GND-J1	GND	DP03-R1-	DP03-R1+	GND-J1	GND
	11	UD	GND	GND-J1	DP03-T2-	DP03-T2+	GND	GND-J1	DP03-R2-	DP03-R2+
	12	GND	DP03-T3-	DP03-T3+	GND-J1	GND	DP03-R3-	DP03-R3+	GND-J1	GND
Data Plane Port 4	13	UD	GND	GND-J1	DP04-T0-	DP04-T0+	GND	GND-J1	DP04-R0-	DP04-R0+
	14	GND	DP04-T1-	DP04-T1+	GND-J1	GND	DP04-R1-	DP04-R1+	GND-J1	GND
	15	Maskable Reset*	GND	GND-J1	DP04-T2-	DP04-T2+	GND	GND-J1	DP04-R2-	DP04-R2+
	16	GND	DP04-T3-	DP04-T3+	GND-J1	GND	DP04-R3-	DP04-R3+	GND-J1	GND

# 3U OpenVPX 5-slot BKP3-DIS05-15.3.2-n Backplane

## J2/P2 Signal Assignments\* (Slots 1-2)

Plug in Module P2-P6	Row G	Row F	Row E		Row D	Row C	Row B		Row A		
			Even	Odd			Even	Odd			
Backplane J2-J6	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a		
X16 using [15:0]	x8 using [7:0]	SEwafer1	GND	GND-J2	LN0-TD-	LN0-TD+	GND	GND-J2	LN0-RD-	LN0-RD+	
			GND	LN1-TD-	LN1-TD+	GND-J2	GND	LN1-RD-	LN1-RD+	GND-J2	GND
		SEwafer3	GND	GND-J2	LN2-TD-	LN2-TD+	GND	GND-J2	LN2-RD-	LN2-RD+	
			GND	LN3-TD-	LN3-TD+	GND-J2	GND	LN3-RD-	LN3-RD+	GND-J2	GND
	x4 using [7:4]	SEwafer5	GND	GND-J2	LN4-TD-	LN4-TD+	GND	GND-J2	LN4-RD-	LN4-RD+	
			GND	LN5-TD-	LN5-TD+	GND-J2	GND	LN5-RD-	LN5-RD+	GND-J2	GND
		SEwafer7	GND	GND-J2	LN6-TD-	LN6-TD+	GND	GND-J2	LN6-RD-	LN6-RD+	
			GND	LN7-TD-	LN7-TD+	GND-J2	GND	LN7-RD-	LN7-RD+	GND-J2	GND
	x8 using [15:8]	SEwafer9	GND	GND-J2	LN8-TD-	LN8-TD+	GND	GND-J2	LN8-RD-	LN8-RD+	
			GND	LN9-TD-	LN9-TD+	GND-J2	GND	LN9-RD-	LN9-RD+	GND-J2	GND
		SEwafer11	GND	GND-J2	LN10-TD-	LN10-TD+	GND	GND-J2	LN10-RD-	LN10-RD+	
			GND	LN11-TD-	LN11-TD+	GND-J2	GND	LN11-RD-	LN11-RD+	GND-J2	GND
		x4 using [15:12]	SEwafer13	GND	GND-J2	LN12-TD-	LN12-TD+	GND	GND-J2	LN12-RD-	LN12-RD+
				GND	LN13-TD-	LN13-TD+	GND-J2	GND	LN13-RD-	LN13-RD+	GND-J2
			SEwafer15	GND	GND-J2	LN14-TD-	LN14-TD+	GND	GND-J2	LN14-RD-	LN14-RD+
				GND	LN15-TD-	LN15-TD+	GND-J2	GND	LN15-RD-	LN15-RD+	GND-J2

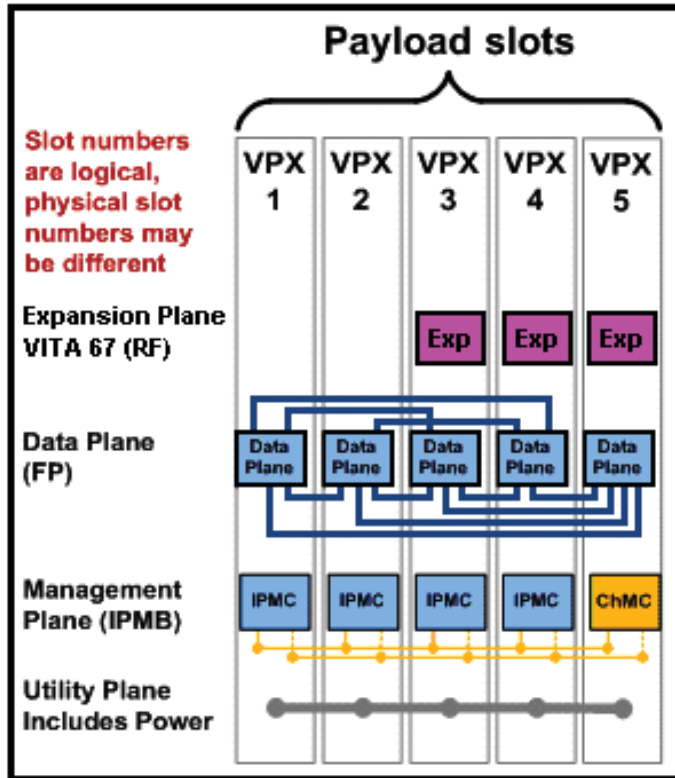
\* Any signal pins pass through the rear

## J2/P2 Signal Assignments (Slots 3-5)

Plug in Module P2-P6	Row G	Row F	Row E		Row D	Row C	Row B		Row A	
			Even	Odd			Even	Odd		
Backplane J2-J6	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a	
X8 using [7:0]	x4 using [3:0]	SEwafer1	GND	GND-J2	LN0-TD-	LN0-TD+	GND	GND-J2	LN0-RD-	LN0-RD+
			GND	LN1-TD-	LN1-TD+	GND-J2	GND	LN1-RD-	LN1-RD+	GND-J2
		SEwafer3	GND	GND-J2	LN2-TD-	LN2-TD+	GND	GND-J2	LN2-RD-	LN2-RD+
			GND	LN3-TD-	LN3-TD+	GND-J2	GND	LN3-RD-	LN3-RD+	GND-J2
	x4 using [7:4]	SEwafer5	GND	GND-J2	LN4-TD-	LN4-TD+	GND	GND-J2	LN4-RD-	LN4-RD+
			GND	LN5-TD-	LN5-TD+	GND-J2	GND	LN5-RD-	LN5-RD+	GND-J2
		SEwafer7	GND	GND-J2	LN6-TD-	LN6-TD+	GND	GND-J2	LN6-RD-	LN6-RD+
			GND	LN7-TD-	LN7-TD+	GND-J2	GND	LN7-RD-	LN7-RD+	GND-J2

# 3U OpenVPX 5-slot BKP3-DIS05-15.3.2-n Backplane

## Backplane Topology

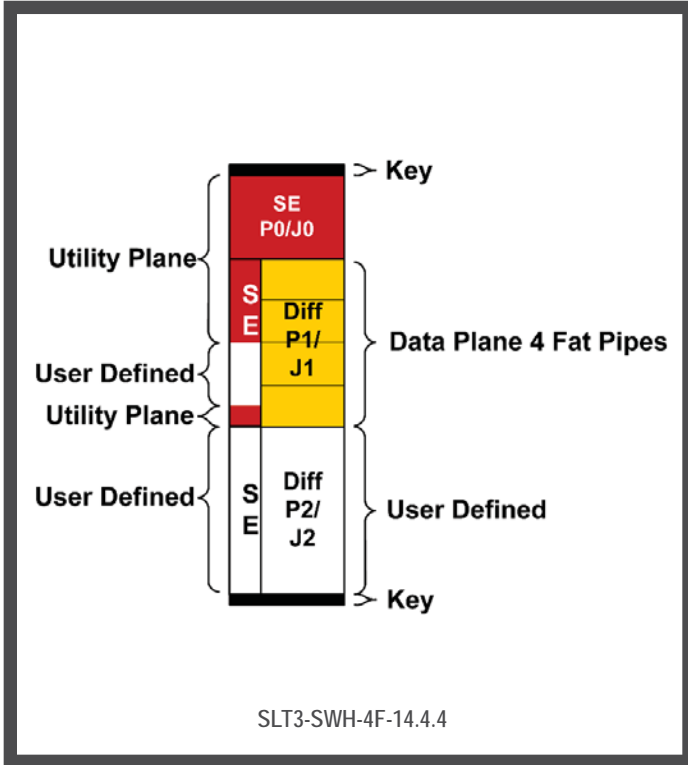


## Backplane Profile

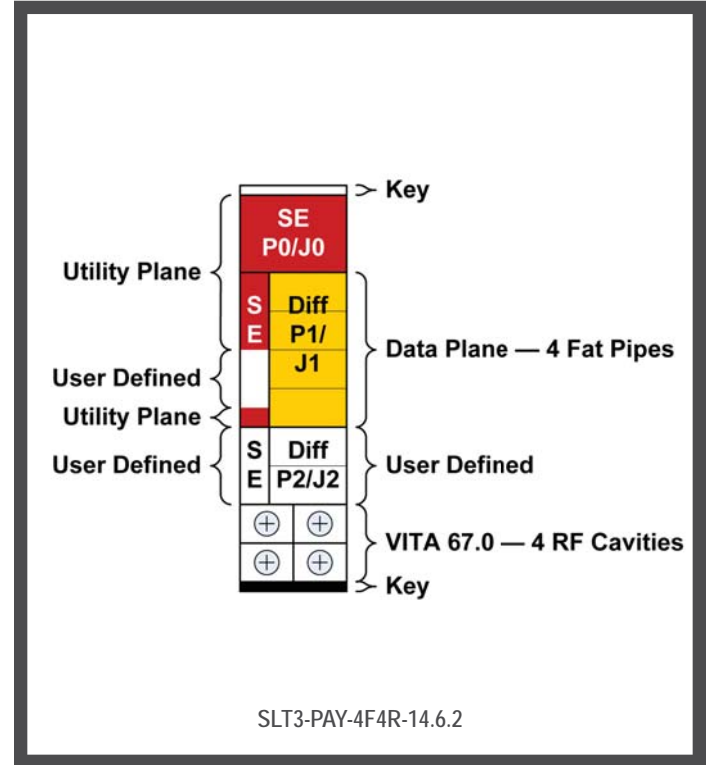
Profile name	Mechanical		Slot Profiles and Section		Channel Gbaud Rate
	Pitch (in)	RTM Conn	Payload Slots 1-2	Payload Slots 3-5	Data Plane
BKP3-DIS05-15.3.2-1	1.0	VITA 46.10	SLT3-SWH-4F-14.4.4	SLT3-PAY-4F4R-14.6.2	3.125
BKP3-DIS05-15.3.2-2	1.0	VITA 46.10	SLT3-SWH-4F-14.4.4	SLT3-PAY-4F4R-14.6.2	5.0
BKP3-DIS05-15.3.2-3	1.0	VITA 46.10	SLT3-SWH-4F-14.4.4	SLT3-PAY-4F4R-14.6.2	6.25

# 3U OpenVPX 5-slot BKP3-DIS05-15.3.2-n Backplane

## Switch Slot Profile



## Payload Slot Profile



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