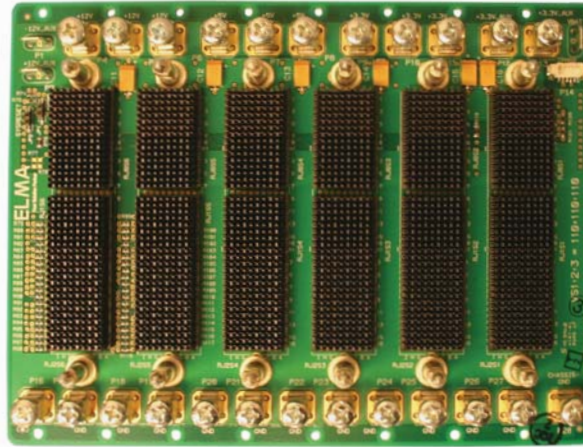


3U OpenVPX 6-slot BKP3-DIS06-15.2.14-n Backplane



Description

Utilizing a twisted-ring topology versus a mesh topology allows for more I/O pins and ability to use mezzanines like XMC. A full mesh topology over 3U VPX would simply take up the vast majority of available pins. In the Elma Bustronic 3U VPX backplane (twisted ring versions), slot 6 has configurable thin pipe links for distributed Gigabit Ethernet to slot 1 through slot 5 and two fat pipes for rear I/O. In slots 1-5 any or all of the P1 thin pipes (x2 channels) assigned to the control channel star can be reconfigured as rear I/O by removing zero ohm SMT shunts. In slots 1-5 all P2 differential pairs are available on the rear side for I/O. In the "AX" part number version, slot 6 is not connected to the other slots, allowing undefined pins for an RTM slot. The only defined pins to the RTM are the 2x thin pipes for the control plane.

The VPX Gigabit Ethernet Control Plane adds a GigE switch, providing a separate star or dual star network for out-of-band communication. This can be particularly important for system management, software and firmware upgrades, and initiating new processes on specific boards.

The Elma Bustronic design solution offers 3.125 to 6.250Gbauds/performance in one PCB. This design provides maximum performance while saving you money. The central switch version of our 3U, 6-slot OpenVPX backplane features a fat pipe expansion plane, a fat pipe Star topology data plane, and an ultra thin pipe for the control plane. It is designed using Nelco-13SI PCB material.

Features

- Compliant to ANSI/VITA 65-2010
- Compliant to the latest VITA 46 Specifications
- High-speed MultiGig connector
- Uses the rugged 3U-160 Eurocard form factor
- Channels A and B are arranged as 2 fat pipes (x4) channels configured as a twisted ring extending from slots 1 to 5
- Provides built in ESD ground protection in every slot
- Versions with or without GigE Control Plane
- Version with slot 6 not connected to other slots for use with RTM

Board Specifications

- 22-layer stripline design
- 2 oz. power and ground
- PCB FR-4 or equivalent
- PCB .212" thick

Mechanical Specifications

- 3U height
- 6 slots
- MultiGig RT-2 connectors

Coming Soon!

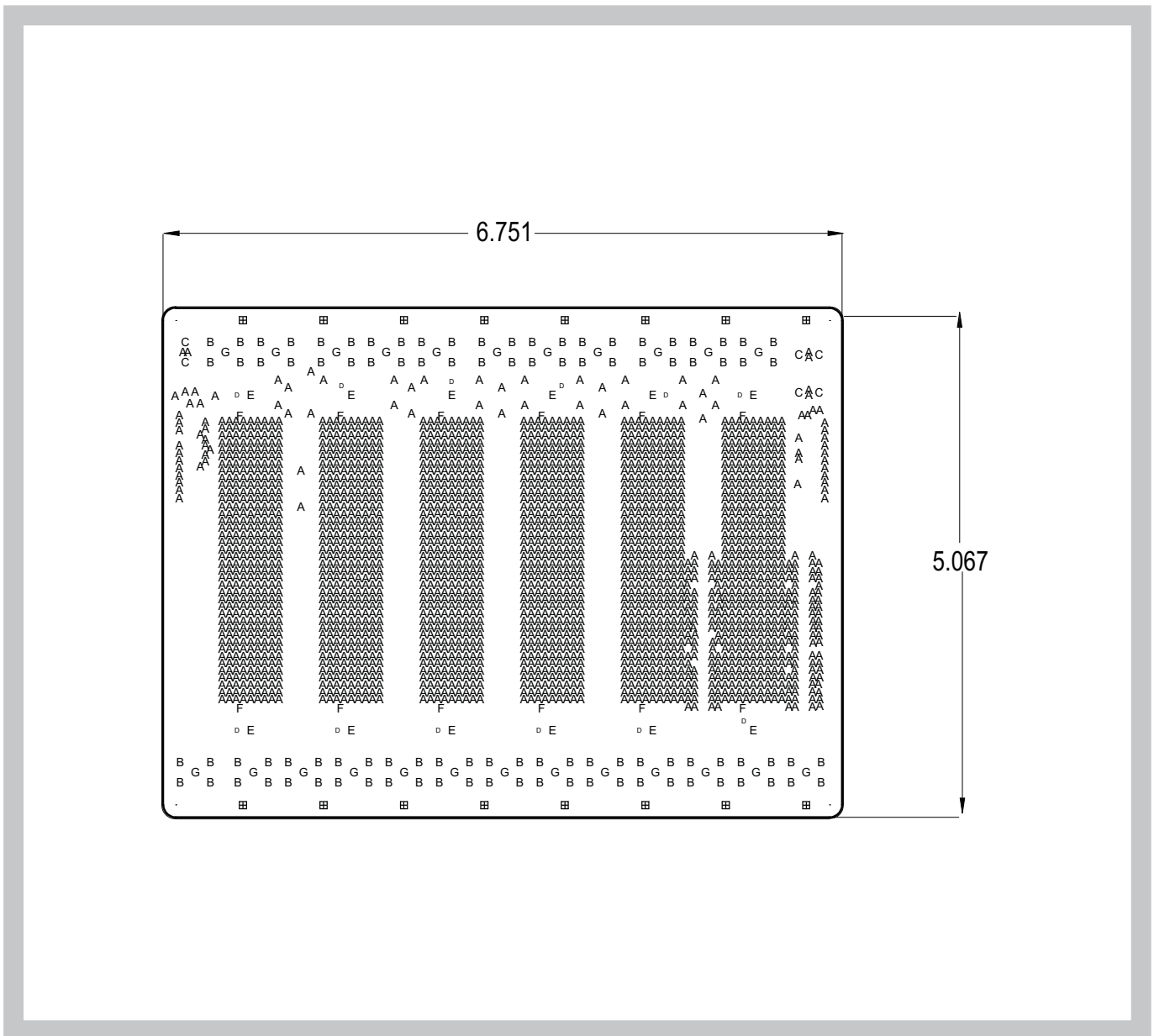
Rear View



Close-up of Power studs and fast-on power blades

3U OpenVPX 6-slot BKP3-DIS06-15.2.14-n Backplane

Line Drawing

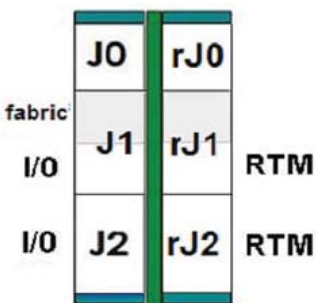


ORDER INFORMATION

| Height | Total Slots | Description | Profile Number | Part Number |
|--------|-------------|--|----------------------|------------------|
| 3U | 6 | VPX twisted ring with configurable Ethernet Control Plane channel Gbaud rate up to 6.25 | BKP3-DIS06-15.2.14-3 | 10VX306SX6-1X11R |
| 3U | 6 | VPX twisted ring with configurable Ethernet Control Plane channel Gbaud rate up to 6.25, no RTM connectors | BKP3-DIS06-15.2.14-3 | 10VX306SX6-1X10R |

3U OpenVPX 6-slot BKP3-DIS06-15.2.14-n Backplane

Connector Positions



J0 Signal Assignments

| | Row I | Row H | Row G | Row F | Row E | Row D | Row C | Row B | Row A |
|---|-------|----------|----------|-------|----------|----------|-----------|-------|-------|
| 1 | Vs1 | Vs1 | Vs1 | Vs1 | No Pad | Vs2 | Vs2 | Vs2 | Vs2 |
| 2 | Vs1 | Vs1 | Vs1 | Vs1 | No Pad | Vs2 | Vs2 | Vs2 | Vs2 |
| 3 | Vs3 | Vs3 | Vs3 | Vs3 | No Pad | Vs3 | Vs3 | Vs3 | Vs3 |
| 4 | GND | SM2 | SM3 | GND | -12V_Aux | GND | SYSRESET* | NVMRO | GND |
| 5 | GND | GAP* | GA4* | GND | 3.3V_Aux | GND | SM0 | SM1 | GND |
| 6 | GND | GA3* | GA2* | GND | +12V_Aux | GND | GA1* | GA0* | GND |
| 7 | TCK | GND | GND | TDO | TDI | GND | GND | TMS | TRST* |
| 8 | GND | REF_CLK- | REF_CLK+ | GND | GND | AUX_CLK- | AUX_CLK+ | GND | GND |

J1 Payload Signal Assignments

| Plug-In Module P1 | Backplane J1 | Row G | Row F | Row E | | Row D | Row C | Row B | | Row A |
|-------------------|---|-----------------|------------|------------|------------|------------|------------|------------|------------|------------|
| | | Row I | Row H | Row G | Row F | Row E | Row D | Row C | Row B | Row A |
| 1 | Data Plane Port 1 X8 x4 / 2x2 / 1x4 | GDiscrete1 | GND | GND-J1 | DP01-TD0- | DP01-TD0+ | GND | GND-J1 | DP01-RD0- | DP01-RD0+ |
| 2 | | GND | DP01-TD1- | DP01-TD1+ | GND-J1 | GND | DP01-RD1- | DP01-RD1+ | GND-J1 | GND |
| 3 | | P1-VBAT | GND | GND-J1 | DP01-TD2- | DP01-TD2+ | GND | GND-J1 | DP01-RD2- | DP01-RD2+ |
| 4 | | GND | DP01-TD3- | DP01-TD3+ | GND-J1 | GND | DP01-RD3- | DP01-RD3+ | GND-J1 | GND |
| 5 | | SYS_CON* | GND | GND-J1 | DP02-TD0- | DP02-TD0+ | GND | GND-J1 | DP02-RD0- | DP02-RD0+ |
| 6 | | GND | DP02-TD1- | DP02-TD1+ | GND-J1 | GND | DP02-RD1- | DP02-RD1+ | GND-J1 | GND |
| 7 | | Reserved | GND | GND-J1 | DP02-TD2- | DP02-TD2+ | GND | GND-J1 | DP02-RD2- | DP02-RD2+ |
| 8 | | GND | DP02-TD3- | DP02-TD3+ | GND-J1 | GND | DP02-RD3- | DP02-RD3+ | GND-J1 | GND |
| 9 | User Defined | UD | GND | GND-J1 | UD | UD | GND | GND-J1 | UD | UD |
| 10 | | GND | UD | UD | GND-J1 | GND | UD | UD | GND-J1 | GND |
| 11 | | UD | GND | GND-J1 | UD | UD | GND | GND-J1 | UD | UD |
| 12 | | GND | UD | UD | GND-J1 | GND | UD | UD | GND-J1 | GND |
| 13 | Control Plane | UD | GND | GND-J4 | CPTp02-DB- | CPTp02-DB+ | GND | GND-J4 | CPTp02-DA- | CPTp02-DA+ |
| 14 | | GND | CPTp02-DD- | CPTp02-DD+ | GND-J4 | GND | CPTp02-DC- | CPTp02-DC+ | GND-J4 | GND |
| 15 | | Makeable Reset* | GND | GND-J4 | CPTp01-DB- | CPTp01-DB+ | GND | GND-J4 | CPTp01-DA- | CPTp01-DA+ |
| 16 | | GND | CPTp01-DD- | CPTp01-DD+ | GND-J4 | GND | CPTp01-DC- | CPTp01-DC+ | GND-J4 | GND |

J1 Switch Signal Assignments

| Plug-In Module P1 | Backplane J1 | Row G | Row F | Row E | | Row D | Row C | Row B | | Row A |
|-------------------|---------------------------|-----------------|------------|------------|------------|------------|------------|------------|------------|------------|
| | | Row I | Row H | Row G | Row F | Row E | Row D | Row C | Row B | Row A |
| 1 | Control Plane Port 1 | GDiscrete1 | GND | GND-J1 | CP01-T0- | CP01-T0+ | GND | GND-J1 | CP01-R0- | CP01-R0+ |
| 2 | | GND | CP01-T1- | CP01-T1+ | GND-J1 | GND | CP01-R1- | CP01-R1+ | GND-J1 | GND |
| 3 | | P1-VBAT | GND | GND-J1 | CP01-T2- | CP01-T2+ | GND | GND-J1 | CP01-R2- | CP01-R2+ |
| 4 | | GND | CP01-T3- | CP01-T3+ | GND-J1 | GND | CP01-R3- | CP01-R3+ | GND-J1 | GND |
| 5 | Control Plane Port 2 | SYS_CON* | GND | GND-J1 | CP02-T0- | CP02-T0+ | GND | GND-J1 | CP02-R0- | CP02-R0+ |
| 6 | | GND | CP02-T1- | CP02-T1+ | GND-J1 | GND | CP02-R1- | CP02-R1+ | GND-J1 | GND |
| 7 | | Reserved | GND | GND-J1 | CP02-T2- | CP02-T2+ | GND | GND-J1 | CP02-R2- | CP02-R2+ |
| 8 | | GND | CP02-T3- | CP02-T3+ | GND-J1 | GND | CP02-R3- | CP02-R3+ | GND-J1 | GND |
| 9 | Control Plane Ports 1 - 8 | UD | GND | GND-J1 | CPTp01-TD- | CPTp01-TD+ | GND | GND-J1 | CPTp01-RD- | CPTp01-RD+ |
| 10 | | GND | CPTp02-TD- | CPTp02-TD+ | GND-J1 | GND | CPTp02-RD- | CPTp02-RD+ | GND-J1 | GND |
| 11 | | UD | GND | GND-J1 | CPTp03-TD- | CPTp03-TD+ | GND | GND-J1 | CPTp03-RD- | CPTp03-RD+ |
| 12 | | GND | CPTp04-TD- | CPTp04-TD+ | GND-J1 | GND | CPTp04-RD- | CPTp04-RD+ | GND-J1 | GND |
| 13 | | UD | GND | GND-J1 | CPTp05-TD- | CPTp05-TD+ | GND | GND-J1 | CPTp05-RD- | CPTp05-RD+ |
| 14 | | GND | CPTp06-TD- | CPTp06-TD+ | GND-J1 | GND | CPTp06-RD- | CPTp06-RD+ | GND-J1 | GND |
| 15 | | Makeable Reset* | GND | GND-J1 | CPTp07-TD- | CPTp07-TD+ | GND | GND-J1 | CPTp07-RD- | CPTp07-RD+ |
| 16 | | GND | CPTp08-TD- | CPTp08-TD+ | GND-J1 | GND | CPTp08-RD- | CPTp08-RD+ | GND-J1 | GND |

3U OpenVPX 6-slot BKP3-DIS06-15.2.14-n Backplane

J2/P2 Signal Assignments* (Slots 1-5)

| Plug in Module P2-P6 | Row G | Row F | Row E | | Row D | Row C | Row B | | Row A |
|----------------------|-----------|----------|----------|----------|----------|----------|----------|----------|----------|
| | Row i | Row h | Even | Odd | Row e | Row d | Even | Odd | Row a |
| 1 | SEwafer1 | GND | GND-J2 | LN0-TD- | LN0-TD+ | GND | GND-J2 | LN0-RD- | LN0-RD+ |
| 2 | GND | LN1-TD- | LN1-TD+ | GND-J2 | GND | LN1-RD- | LN1-RD+ | GND-J2 | GND |
| 3 | SEwafer3 | GND | GND-J2 | LN2-TD- | LN2-TD+ | GND | GND-J2 | LN2-RD- | LN2-RD+ |
| 4 | GND | LN3-TD- | LN3-TD+ | GND-J2 | GND | LN3-RD- | LN3-RD+ | GND-J2 | GND |
| 5 | SEwafer5 | GND | GND-J2 | LN4-TD- | LN4-TD+ | GND | GND-J2 | LN4-RD- | LN4-RD+ |
| 6 | GND | LN5-TD- | LN5-TD+ | GND-J2 | GND | LN5-RD- | LN5-RD+ | GND-J2 | GND |
| 7 | SEwafer7 | GND | GND-J2 | LN6-TD- | LN6-TD+ | GND | GND-J2 | LN6-RD- | LN6-RD+ |
| 8 | GND | LN7-TD- | LN7-TD+ | GND-J2 | GND | LN7-RD- | LN7-RD+ | GND-J2 | GND |
| 9 | SEwafer9 | GND | GND-J2 | LN8-TD- | LN8-TD+ | GND | GND-J2 | LN8-RD- | LN8-RD+ |
| 10 | GND | LN9-TD- | LN9-TD+ | GND-J2 | GND | LN9-RD- | LN9-RD+ | GND-J2 | GND |
| 11 | SEwafer11 | GND | GND-J2 | LN10-TD- | LN10-TD+ | GND | GND-J2 | LN10-RD- | LN10-RD+ |
| 12 | GND | LN11-TD- | LN11-TD+ | GND-J2 | GND | LN11-RD- | LN11-RD+ | GND-J2 | GND |
| 13 | SEwafer13 | GND | GND-J2 | LN12-TD- | LN12-TD+ | GND | GND-J2 | LN12-RD- | LN12-RD+ |
| 14 | GND | LN13-TD- | LN13-TD+ | GND-J2 | GND | LN13-RD- | LN13-RD+ | GND-J2 | GND |
| 15 | SEwafer15 | GND | GND-J2 | LN14-TD- | LN14-TD+ | GND | GND-J2 | LN14-RD- | LN14-RD+ |
| 16 | GND | LN15-TD- | LN15-TD+ | GND-J2 | GND | LN15-RD- | LN15-RD+ | GND-J2 | GND |

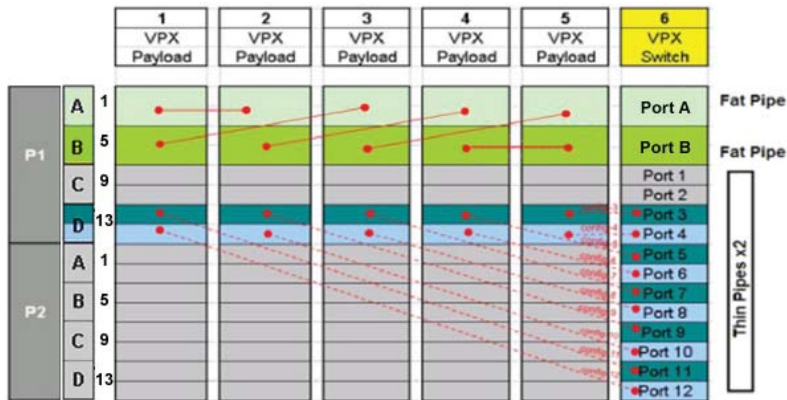
* Any signal pins pass through the rear

J2/P2 Switch Signal Assignments (Slot 6)

| Plug-In Module P2 | Row G | Row F | Row E | | Row D | Row C | Row B | | Row A |
|-------------------|-------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| | Row i | Row h | Even | Odd | Row e | Row d | Even | Odd | Row a |
| 1 | UD | GND | GND-J2 | CPUTP09-TD- | CPUTP09-TD+ | GND | GND-J2 | CPUTP09-RD- | CPUTP09-RD+ |
| 2 | GND | CPUTP10-TD- | CPUTP10-TD+ | GND-J2 | GND | CPUTP10-RD- | CPUTP10-RD+ | GND-J2 | GND |
| 3 | UD | GND | GND-J2 | CPUTP11-TD- | CPUTP11-TD+ | GND | GND-J2 | CPUTP11-RD- | CPUTP11-RD+ |
| 4 | GND | CPUTP12-TD- | CPUTP12-TD+ | GND-J2 | GND | CPUTP12-RD- | CPUTP12-RD+ | GND-J2 | GND |
| 5 | UD | GND | GND-J2 | CPUTP13-TD- | CPUTP13-TD+ | GND | GND-J2 | CPUTP13-RD- | CPUTP13-RD+ |
| 6 | GND | CPUTP14-TD- | CPUTP14-TD+ | GND-J2 | GND | CPUTP14-RD- | CPUTP14-RD+ | GND-J2 | GND |
| 7 | UD | GND | GND-J2 | CPUTP15-TD- | CPUTP15-TD+ | GND | GND-J2 | CPUTP15-RD- | CPUTP15-RD+ |
| 8 | GND | CPUTP16-TD- | CPUTP16-TD+ | GND-J2 | GND | CPUTP16-RD- | CPUTP16-RD+ | GND-J2 | GND |
| 9 | UD | GND | GND-J2 | CPUTP17-TD- | CPUTP17-TD+ | GND | GND-J2 | CPUTP17-RD- | CPUTP17-RD+ |
| 10 | GND | CPUTP18-TD- | CPUTP18-TD+ | GND-J2 | GND | CPUTP18-RD- | CPUTP18-RD+ | GND-J2 | GND |
| 11 | UD | GND | GND-J2 | CPUTP19-TD- | CPUTP19-TD+ | GND | GND-J2 | CPUTP19-RD- | CPUTP19-RD+ |
| 12 | GND | CPUTP20-TD- | CPUTP20-TD+ | GND-J2 | GND | CPUTP20-RD- | CPUTP20-RD+ | GND-J2 | GND |
| 13 | UD | GND | GND-J2 | CPUTP21-TD- | CPUTP21-TD+ | GND | GND-J2 | CPUTP21-RD- | CPUTP21-RD+ |
| 14 | GND | CPUTP22-TD- | CPUTP22-TD+ | GND-J2 | GND | CPUTP22-RD- | CPUTP22-RD+ | GND-J2 | GND |
| 15 | UD | GND | GND-J2 | CPUTP23-TD- | CPUTP23-TD+ | GND | GND-J2 | CPUTP23-RD- | CPUTP23-RD+ |
| 16 | GND | CPUTP24-TD- | CPUTP24-TD+ | GND-J2 | GND | CPUTP24-RD- | CPUTP24-RD+ | GND-J2 | GND |

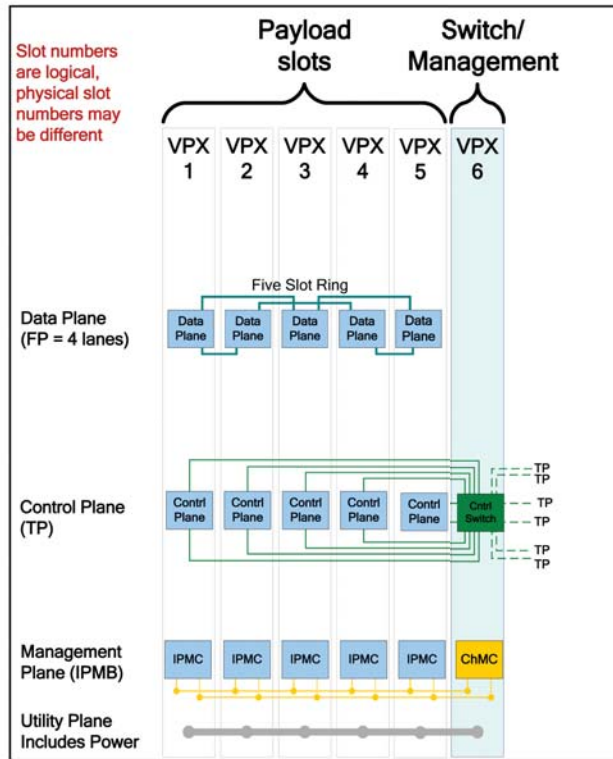
3U OpenVPX 6-slot BKP3-DIS06-15.2.14-n Backplane

Port Mapping



Ports A and B in slots 1-5 are fat pipes implemented via one twisted ring as the primary VITA 46 fabric. The fabric may be 10G Ethernet (10GBASE KX-4), sRIO, or PCIe. Slot 6 is a switch slot for a thin pipe, redundant dual star, or distributed GigE per VITA 46.20. The GigE is configurable at each of the slots 1-5 so that any individual slot could utilize ports in J1 rows 9-12 for rear I/O if desired. Port A and port B in slot 6 have 10G Ethernet rear I/O.

Backplane Topology

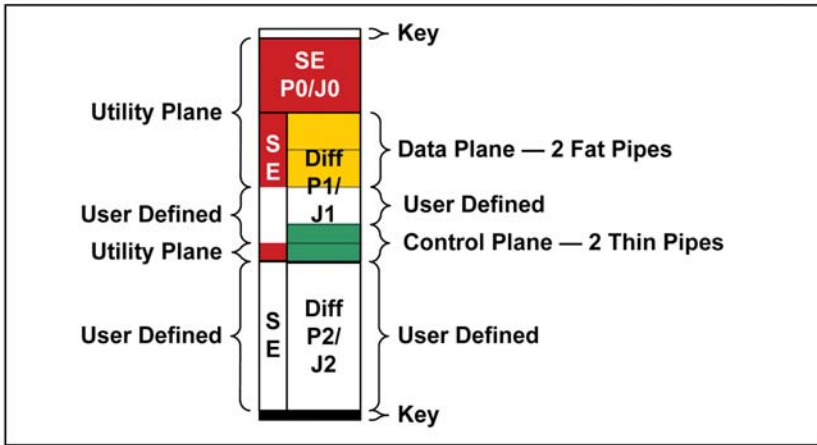


Backplane Profile

| Profile name | Mechanical | | Slot Profiles and Section | | Channel Gbaud Rate | |
|----------------------|------------|------------|---------------------------|---------------------|--------------------|------------|
| | Pitch (in) | RTM Conn | Payload | Switch | Control Plane | Data Plane |
| BKP3-DIS06-15.2.14-1 | 1.0 | VITA 46.10 | SLT3-PAY-2F2T-14.2.5 | SLT3-SWH-16T-14.4.6 | 1.25 | 3.125 |
| BKP3-DIS06-15.2.14-2 | 1.0 | VITA 46.10 | SLT3-PAY-2F2T-14.2.5 | SLT3-SWH-16T-14.4.6 | 1.25 | 5.0 |
| BKP3-DIS06-15.2.14-3 | 1.0 | VITA 46.10 | SLT3-PAY-2F2T-14.2.5 | SLT3-SWH-16T-14.4.6 | 1.25 | 6.25 |

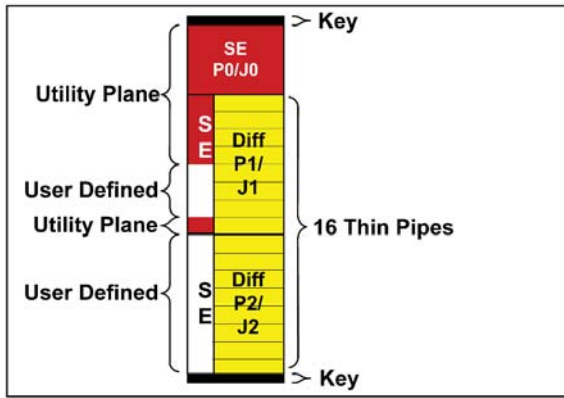
3U OpenVPX 6-slot BKP3-DIS06-15.2.14-n Backplane

Payload Slot Profile



SLT3-PAY-2F2T-14.2.5

Switch Slot Profile



SLT3-SWH-16T-14.4.6

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- System Platforms – need a chassis for your backplane?
- VPX Embedded Computing Products – SBCs, Switches, Storage, and More



Did you know we also offer with this OpenVPX backplane?

- VPX Extenders, load boards, RTMs, test modules
- Thermal or backplane simulation/test, paint/silkscreen, customization, integration