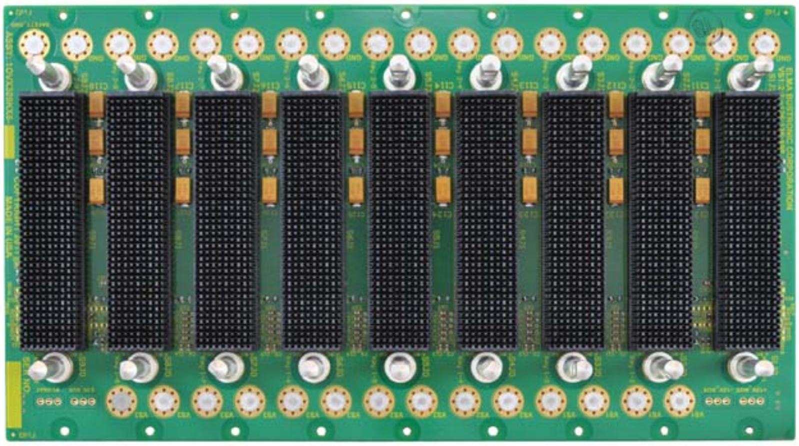
3U OpenVPX 9-slot BKP3-CEN09-15.2.17-n Backplanes - With and Without Expansion Control Planes



Description

Elma Bustronic offers two versions of the BKP3-CEN09-15.2.17-n Backplane: one with an expansion control plane and one without. Designed to VITA 65 design principles, the 9-slot OpenVPX backplane features a centralized routing topology. The switch slot is connected to slots 1, 5, 6, 7, 8, and 9. Slots 1-3 are also connected on the data plane. The version with the expansion plane have those signals going across slots 6-9. Contiguous groups of slots can have their maskable reset pin joined via jumpers within a provided backplane header.

Features

- Version with expansion plane compliant to VITA 65 specification. Version without expansion plane is VITA 65 compatible.
- Uses the rugged 3U-160 Eurocard form factor
- High-speed MultiGig connector
- Version with expansion plane in slots 5-8
- Provides built in ESD ground protection in every slot

Board Specifications

- 16 (KX version), 18 (KY version)
- 2 oz. power and ground
- PCB FR-4
- PCB .213" thick

Mechanical Specifications

- 3U height
- 9 slots

Profile name	Mechanical		Slot Profiles and Section				Channel Gbaud Rate		
	Pitch (in)	RTM Conn	Slot 1 Payload	Slots 2-3 Payload	Slots 5-9 Payload	Slot 4 Switch	Control Plane	Data Plane	Expan Plane
BKP3-CEN09-15.2.17-1	1.0	VITA 46.10	SLT3-PAY-3F2U-14.2.13	SLT3-PAY-1F2U-14.2.12	SLT3-PAY-1F2F2U-14.2.2	SLT3-SWH-6F8U-14.4.9	1.25	3.125	5.0
BKP3-CEN09-15.2.17-2	1.0	VITA 46.10	SLT3-PAY-3F2U-14.2.13	SLT3-PAY-1F2U-14.2.12	SLT3-PAY-1F2F2U-14.2.2	SLT3-SWH-6F8U-14.4.9	1.25	5.0	5.0
BKP3-CEN09-15.2.17-3	1.0	VITA 46.10	SLT3-PAY-3F2U-14.2.13	SLT3-PAY-1F2U-14.2.12	SLT3-PAY-1F2F2U-14.2.2	SLT3-SWH-6F8U-14.4.9	1.25	6.25	5.0

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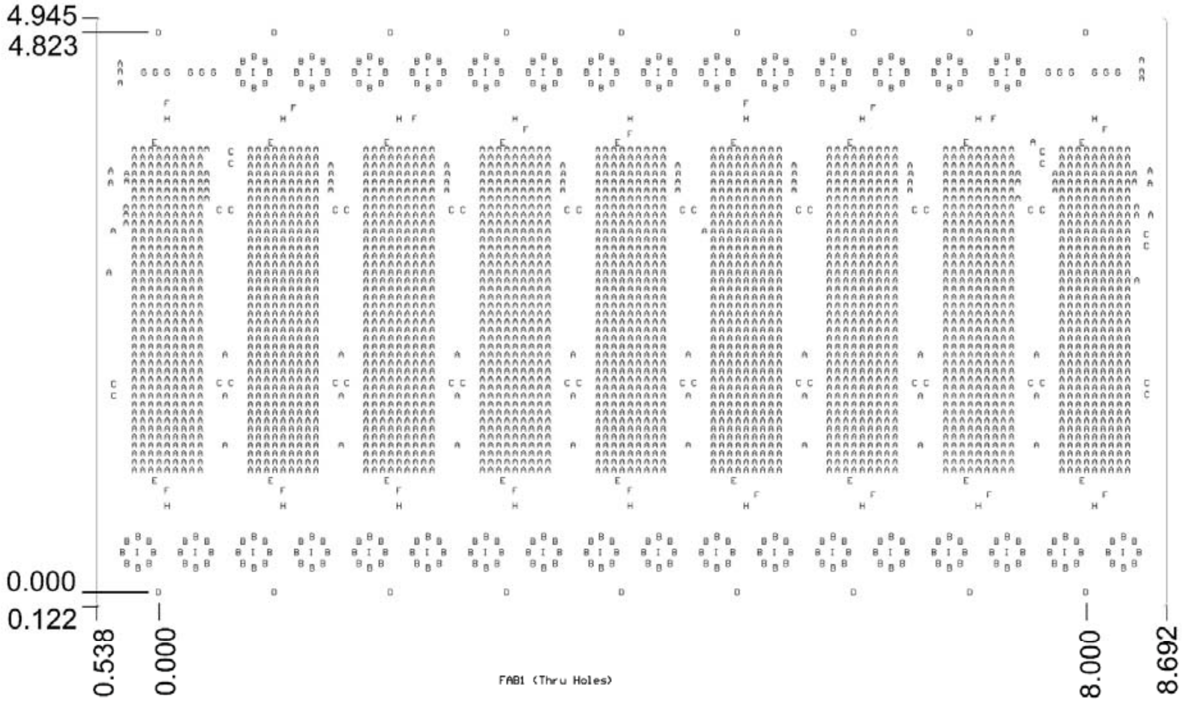
Line Drawing



ORDER INFORMATION

Height	Total Slots	Description	Profile Number	Part Number
3U	9	VPX central switch with expansion plane, channel Gbaud rate up to 6.25	BKP3-CENO9-15.2-17-3	1OVX309KX6-1X11R
3U	9	VPX central switch with expansion plane, channel Gbaud rate up to 6.25, no RTM connectors	BKP3-CENO9-15.2-17-3	1OVX309KX6-1X10R
3U	9	VPX central switch without expansion plane, channel Gbaud rate up to 6.25	BKP3-CENO9-15.2-17-3	1OVX309KY6-1X11R
3U	9	VPX central switch without expansion plane, channel Gbaud rate up to 6.25, no RTM connectors	BKP3-CENO9-15.2-17-3	1OVX309KY6-1X10R

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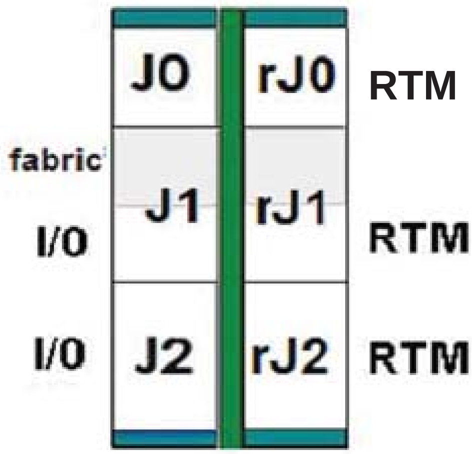
Connector Positions



J0 Signal Assignments

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

J1/P1 Signal Assignments for Slots 2 & 3

Plug-in module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1 / 1x4 / 2x2 / 4x1	GDiscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2		GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4		GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	User Defined	SYS_CON*	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
6		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
7		Reserved	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
8		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
9		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15	Control Plane	Maskable Reset*	GND	GND-J1	CPutp02-TD-	CPutp02-TD+	GND	GND-J1	CPutp02-RD-	CPutp02-RD+
16		GND	CPutp01-TD-	CPutp01-TD+	GND-J1	GND	CPutp01-RD-	CPutp01-RD+	GND-J1	GND

J1/P1 Signal Assignments for Slots 6-9

Plug-in Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1 / x4 / 2x2 / 4x1	GDiscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2		GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4		GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Expan. Plane Port 1 / x8 / x4 / 2x2 / 4x1	SYS_CON*	GND	GND-J1	EP00-TD-	EP00-TD+	GND	GND-J1	EP00-RD-	EP00-RD+
6		GND	EP01-TD-	EP01-TD+	GND-J1	GND	EP01-RD-	EP01-RD+	GND-J1	GND
7		Reserved	GND	GND-J1	EP02-TD-	EP02-TD+	GND	GND-J1	EP02-RD-	EP02-RD+
8		GND	EP03-TD-	EP03-TD+	GND-J1	GND	EP03-RD-	EP03-RD+	GND-J1	GND
9	Expan. Plane Port 2 / x4 / 2x2 / 4x1	UD	GND	GND-J1	EP04-TD-	EP04-TD+	GND	GND-J1	EP04-RD-	EP04-RD+
10		GND	EP05-TD-	EP05-TD+	GND-J1	GND	EP05-RD-	EP05-RD+	GND-J1	GND
11		UD	GND	GND-J1	EP06-TD-	EP06-TD+	GND	GND-J1	EP06-RD-	EP06-RD+
12		GND	EP07-TD-	EP07-TD+	GND-J1	GND	EP07-RD-	EP07-RD+	GND-J1	GND
13	User Defined	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15	Control Plane	Maskable Reset*	GND	GND-J1	CPutp02-TD-	CPutp02-TD+	GND	GND-J1	CPutp02-RD-	CPutp02-RD+
16		GND	CPutp01-TD-	CPutp01-TD+	GND-J1	GND	CPutp01-RD-	CPutp01-RD+	GND-J1	GND

*J2 slots 1-3 and 5-9 are user defined

J1/P1 Signal Assignments for Slot 1

Plug-in module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1 / X8 / x4 / 2x2 / 4x1	GDiscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2		GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4		GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Data Plane Port 2 / x4 / 2x2 / 4x1	SYS_CON*	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
6		GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
8		GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
9	User Defined	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15	Control Plane	Maskable Reset*	GND	GND-J1	CPutp02-TD-	CPutp02-TD+	GND	GND-J1	CPutp02-RD-	CPutp02-RD+
16		GND	CPutp01-TD-	CPutp01-TD+	GND-J1	GND	CPutp01-RD-	CPutp01-RD+	GND-J1	GND

J1/P1 Signal Assignments for Slot 4

Plug-in Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2		GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4		GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
6		GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
8		GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
9	Data Plane Port 3	UD	GND	GND-J1	DP03-TD0-	DP03-TD0+	GND	GND-J1	DP03-RD0-	DP03-RD0+
10		GND	DP03-TD1-	DP03-TD1+	GND-J1	GND	DP03-RD1-	DP03-RD1+	GND-J1	GND
11		UD	GND	GND-J1	DP03-TD2-	DP03-TD2+	GND	GND-J1	DP03-RD2-	DP03-RD2+
12		GND	DP03-TD3-	DP03-TD3+	GND-J1	GND	DP03-RD3-	DP03-RD3+	GND-J1	GND
13	Data Plane Port 4	UD	GND	GND-J1	DP04-TD0-	DP04-TD0+	GND	GND-J1	DP04-RD0-	DP04-RD0+
14		GND	DP04-TD1-	DP04-TD1+	GND-J1	GND	DP04-RD1-	DP04-RD1+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	DP04-TD2-	DP04-TD2+	GND	GND-J1	DP04-RD2-	DP04-RD2+
16		GND	DP04-TD3-	DP04-TD3+	GND-J1	GND	DP04-RD3-	DP04-RD3+	GND-J1	GND

J2/P2 Signal Assignments for Slot 4

Plug-in Module P2		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J2		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 5	UD	GND	GND-J2	DP05-TD0-	DP05-TD0+	GND	GND-J2	DP05-RD0-	DP05-RD0+
2		GND	DP05-TD1-	DP05-TD1+	GND-J2	GND	DP05-RD1-	DP05-RD1+	GND-J2	GND
3		UD	GND	GND-J2	DP05-TD2-	DP05-TD2+	GND	GND-J2	DP05-RD2-	DP05-RD2+
4		GND	DP05-TD3-	DP05-TD3+	GND-J2	GND	DP05-RD3-	DP05-RD3+	GND-J2	GND
5	Data Plane Port 6	UD	GND	GND-J2	DS01-TD0-	DS01-TD0+	GND	GND-J2	DS01-RD0-	DS01-RD0+
6		GND	DS01-TD1-	DS01-TD1+	GND-J2	GND	DS01-RD1-	DS01-RD1+	GND-J2	GND
7		UD	GND	GND-J2	DS01-TD2-	DS01-TD2+	GND	GND-J2	DS01-RD2-	DS01-RD2+
8		GND	DS01-TD3-	DS01-TD3+	GND-J2	GND	DS01-RD3-	DS06-RD3+	GND-J2	GND
9	Control Plane Ports 1 - 8	UD	GND	GND-J2	CSutp01-TD-	CSutp01-TD+	GND	GND-J2	CSutp01-RD-	CSutp01-RD+
10		GND	CPutp05-TD-	CPutp05-TD+	GND-J2	GND	CPutp05-RD-	CPutp05-RD+	GND-J2	GND
11		UD	GND	GND-J2	CPutp04-TD-	CPutp04-TD+	GND	GND-J2	CPutp04-RD-	CPutp04-RD+
12		GND	CPutp03-TD-	CPutp03-TD+	GND-J2	GND	CPutp03-RD-	CPutp03-RD+	GND-J2	GND
13		UD	GND	GND-J2	CPutp02-TD-	CPutp02-TD+	GND	GND-J2	CPutp02-RD-	CPutp02-RD+
14		GND	CPutp01-TD-	CPutp01-TD+	GND-J2	GND	CPutp01-RD-	CPutp01-RD+	GND-J2	GND
15		UD	GND	GND-J2	Cputp07-TD-	Cputp07-TD+	GND	GND-J2	Cputp07-RD-	Cputp07-RD+
16		GND	CPutp06-TD-	CPutp06-TD+	GND-J2	GND	CPutp06-RD-	CPutp06-RD+	GND-J2	GND

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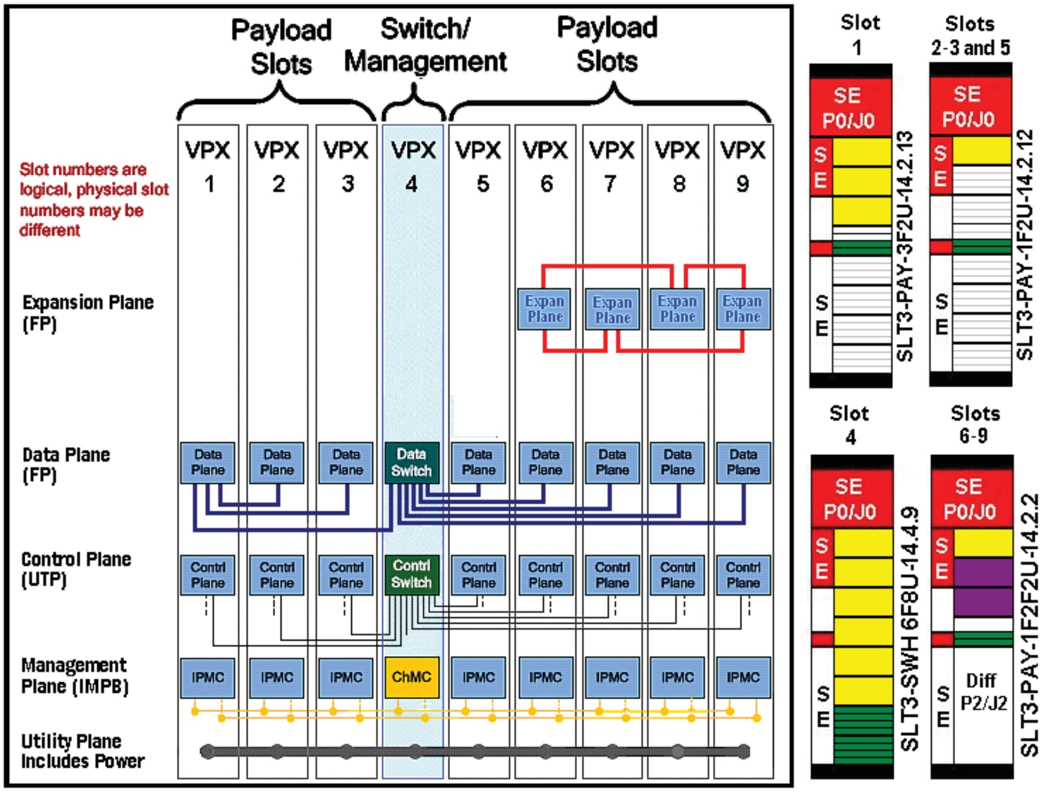
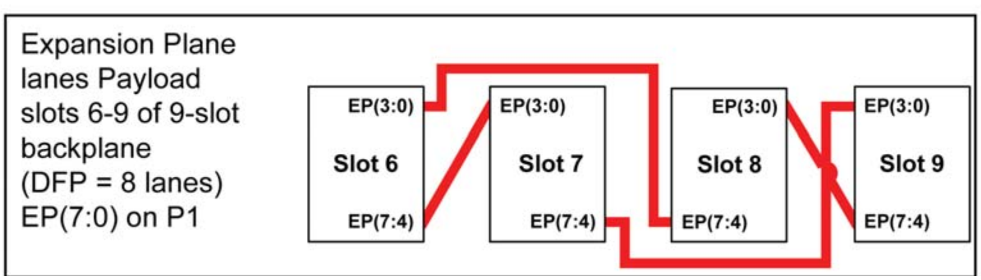
Backplane Topology



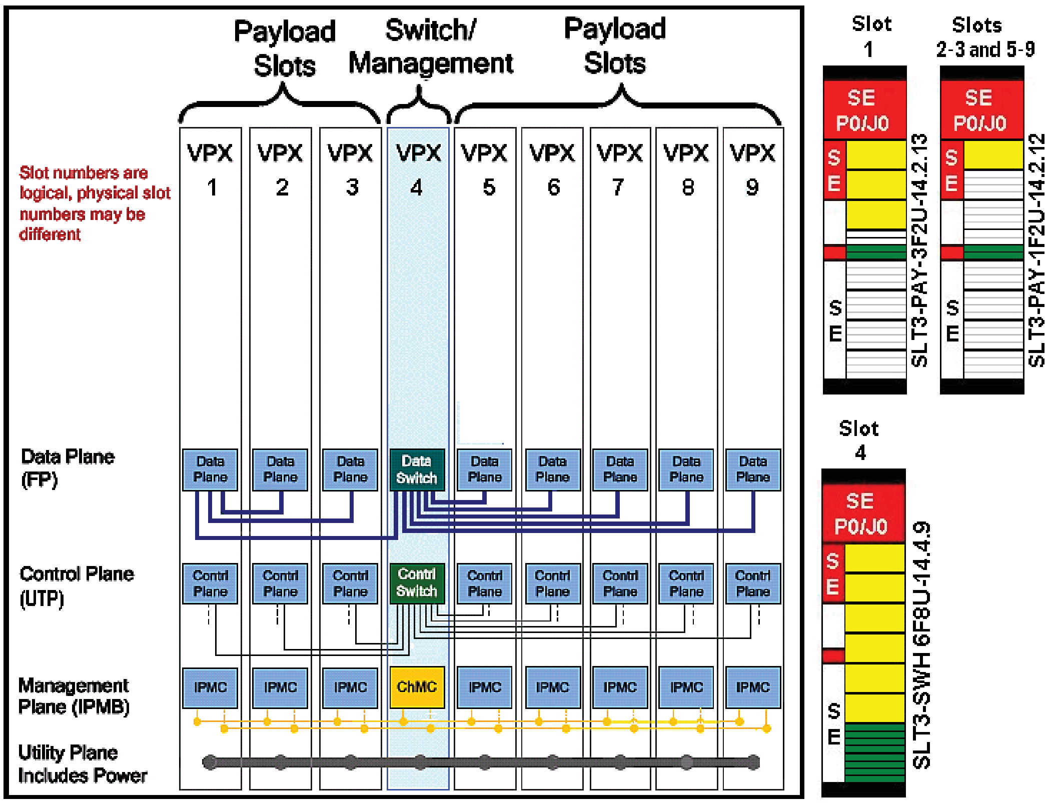
BKP3-CEN09-15.2-17-n with switch in slot 4 with expansion plane

Expansion Planes



3U OpenVPX 9-slot BKP3-CEN09-15.2.17-n Backplanes - With and Without Expansion Control Planes

Backplane Topology



BKP3-CEN09-15.2-17-n with switch in slot 4 without expansion plane

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