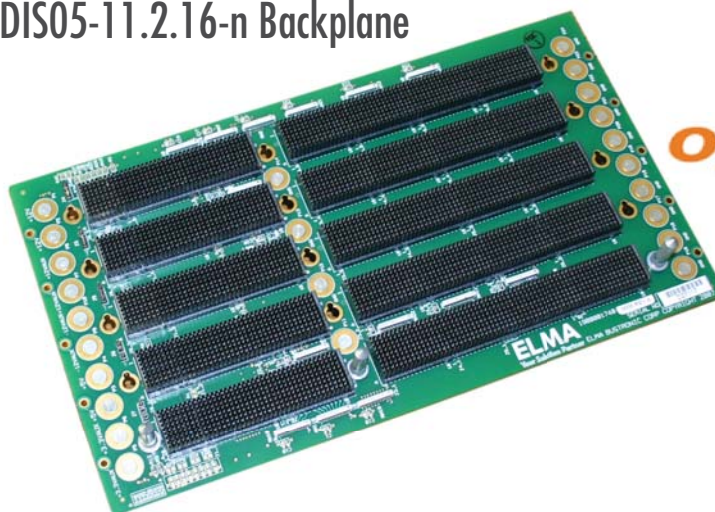


6U OpenVPX 5-Slot BKP6-DIS05-11.2.16-n Backplane



OpenVPX

Description

VITA 46.0 is the core document for VPX and applies to all of the subsidiary documents. Therefore because our backplanes meet the requirements of VITA 46.0 they are designed to support all of the subsidiary documents for sRIO, PCI Express, Ethernet or Infiniband. Note that VITA 46.1 and 46.20 specify additional signals that are not present in a backplane unless specifically mentioned in its description.

While maintaining backward compatibility with legacy VME technology via preservation of the VMEbus 6U mechanical form factor and through-mapping of the current VMEbus signals to the VITA 46 connectors, the VITA 46 technology brings the following features to reality while maintaining ability to inter-operate with existing VME technology boards:

- Vastly increased high-speed serial I/O support for such needs as digital video, mass storage interconnects (e.g. SATA) and FPGA interconnects (e.g. RocketIO).
- Support for high-speed switched serial fabrics with performance up to 10 Gbps.
- Support for cost-reducing two-level maintenance by providing an Electrostatic Discharge (ESD) protection mechanism and board covers.
- Support of distributed switching that eliminates the need for dedicated switch card slots.
- Support for VITA 42 mezzanine sites with high speed I/O.

Elma is the leader in VITA 46/48 VPX products. Our experts developed the industry's first VPX backplane and proposed the first VME pinouts to the VITA 46 subcommittee. Since then, Elma has developed various VPX configurations with and without legacy VME64x slots.

OpenVPX provides an easier way to ensure interoperability between VPX systems. The VPX Modules and Slots across the backplanes have been given definitions so that similar Modules will work within certain Slot configurations. The backplane configurations have been defined to show the collection of slot profiles it entails, including information on the data rate, routing topology, and fabric used. Now, a daughtercard Module from "X" company can be used in the same backplane slot as "Y" company's, as they have the same defined Module profile for that slot. The OpenVPX V1.0 Specification, developed by VITA members, has been turned over to the VSO in October 2009 as VITA 65 for final comment, ballot, and ratification as a standard.

Features

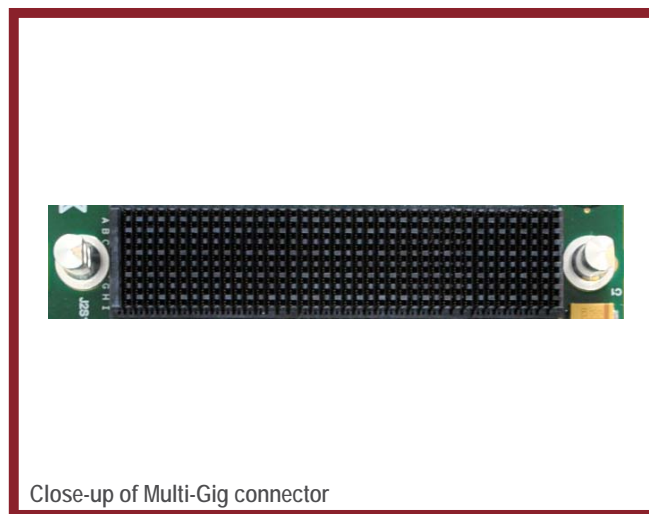
- Compliant to ANSI/VITA VITA 65 Rev 1.0
- Compliant to the latest VITA 46 Specifications
- High-speed Multi-gig connector
- Rugged Eurocard form factor in 6U height
- Provides built in ESD ground protection in every slot
- Signal Integrity studies available upon request
- Hybrid versions are available

Board Specifications

- 18 layer stripline design
- 2 oz. power and ground
- PCB FR-4 or equivalent
- PCB .212" thick

Mechanical Specifications

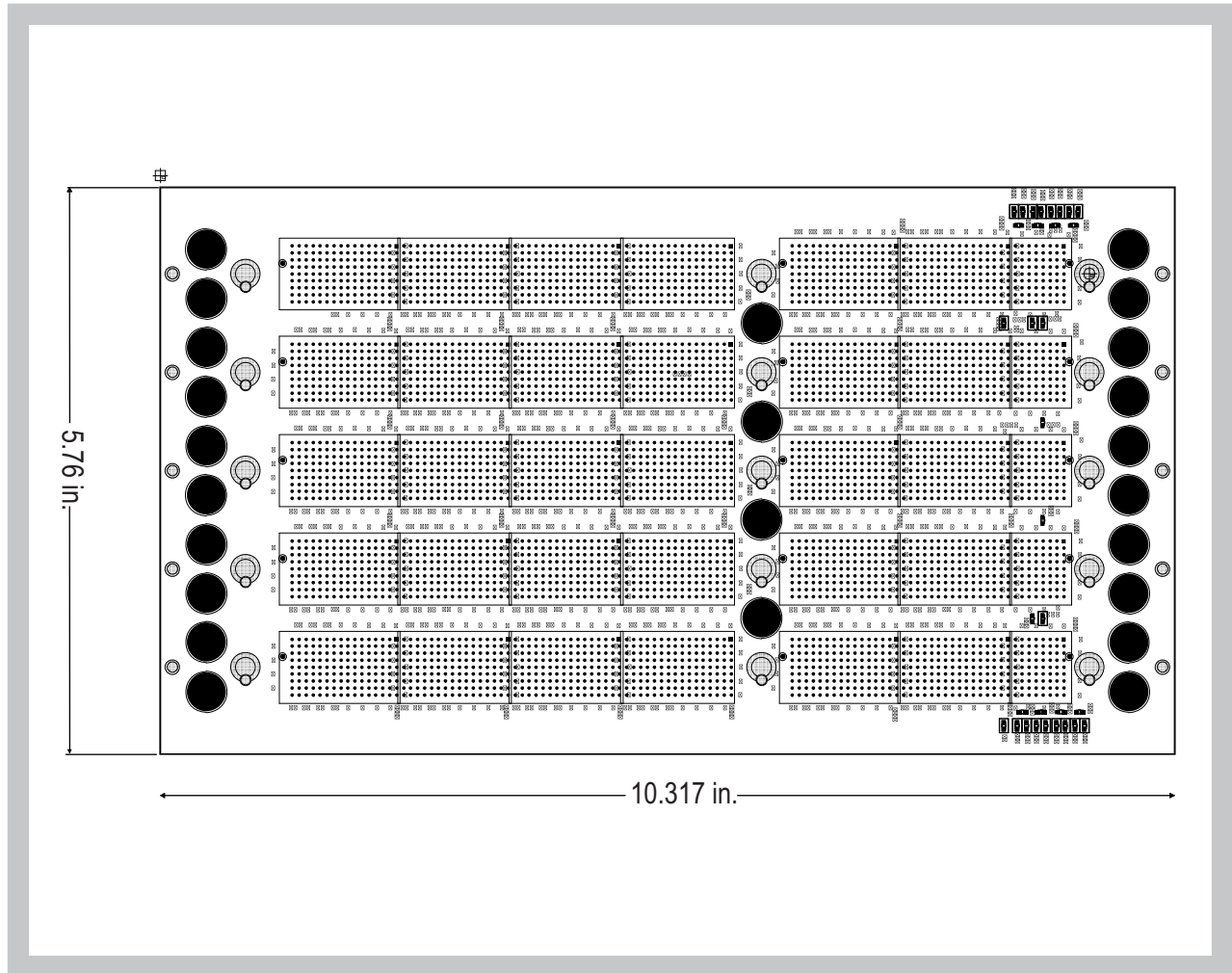
- 6U height
- 5 slots
- MultiGig RT-2 connectors



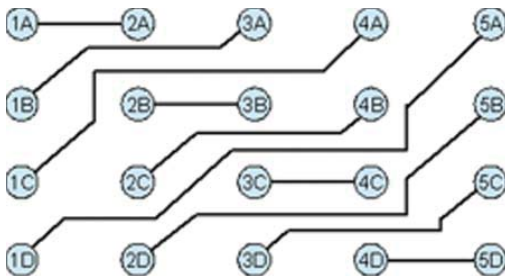
Close-up of Multi-Gig connector

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Line Drawing



Connectivity Chart

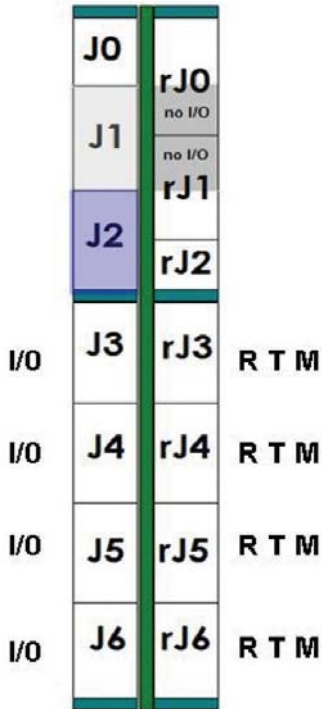


Order Information

Height	Total Slots	Description	Profile Number	Part Number
6U	5	VPX mesh, 4 lane fat pipe, same cost-effective PCB used for 3.125 to 6.25 Gbaud speeds	BKP6-DIS05-11.2.16-1	10VX605MX6-1X01R
6U	5	VPX mesh, 4 lane fat pipe, no RTM connectors, same cost-effective PCB used for 3.125 to 6.25 Gbaud speeds	BKP6-DIS05-11.2.16-1	10VX605MX6-1X00R

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Connector Positions



J0 Signal Assignments

	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

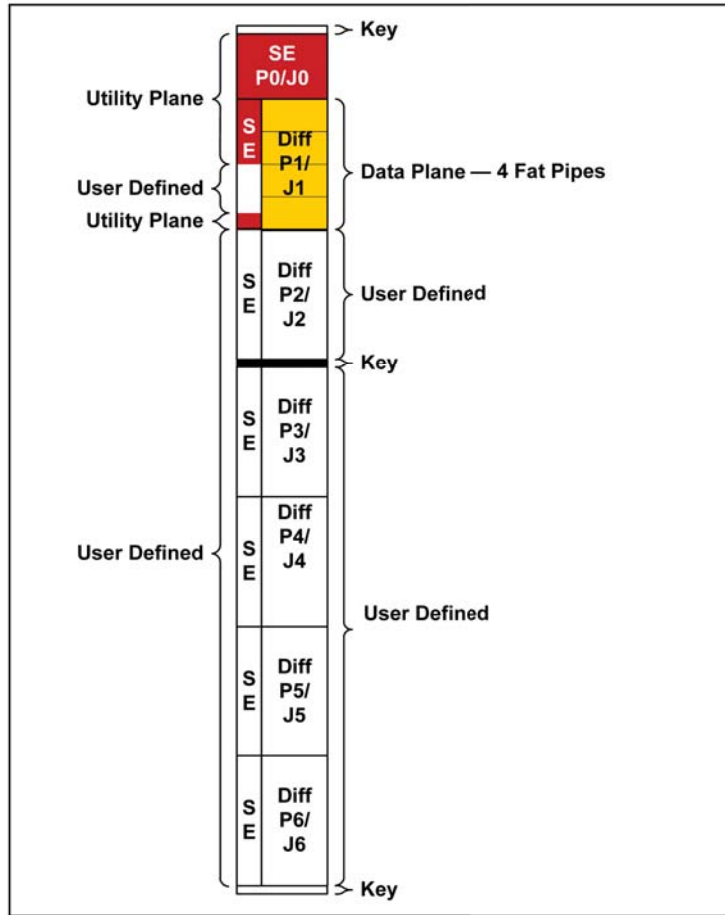
J1/P1 Signal Assignments

Plug-In Module P1	Row G	Row F	Row E		Row D	Row C	Row B		Row A	
			Even	Odd			Even	Odd		
Bplane J1	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a	
Data Plane Port 1	1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
	2	GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
	3	P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
Data Plane Port 2	4	GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
	5	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
	6	GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
	7	Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
Data Plane Port 3	8	GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
	9	UD	GND	GND-J1	DP03-T0-	DP03-T0+	GND	GND-J1	DP03-R0-	DP03-R0+
	10	GND	DP03-T1-	DP03-T1+	GND-J1	GND	DP03-R1-	DP03-R1+	GND-J1	GND
Data Plane Port 4	11	UD	GND	GND-J1	DP03-T2-	DP03-T2+	GND	GND-J1	DP03-R2-	DP03-R2+
	12	GND	DP03-T3-	DP03-T3+	GND-J1	GND	DP03-R3-	DP03-R3+	GND-J1	GND
	13	UD	GND	GND-J1	DP04-T0-	DP04-T0+	GND	GND-J1	DP04-R0-	DP04-R0+
	14	GND	DP04-T1-	DP04-T1+	GND-J1	GND	DP04-R1-	DP04-R1+	GND-J1	GND
Data Plane Port 4	15	Maskable Reset*	GND	GND-J1	DP04-T2-	DP04-T2+	GND	GND-J1	DP04-R2-	DP04-R2+
	16	GND	DP04-T3-	DP04-T3+	GND-J1	GND	DP04-R3-	DP04-R3+	GND-J1	GND

J2-J6 Signal Assignments = User Defined

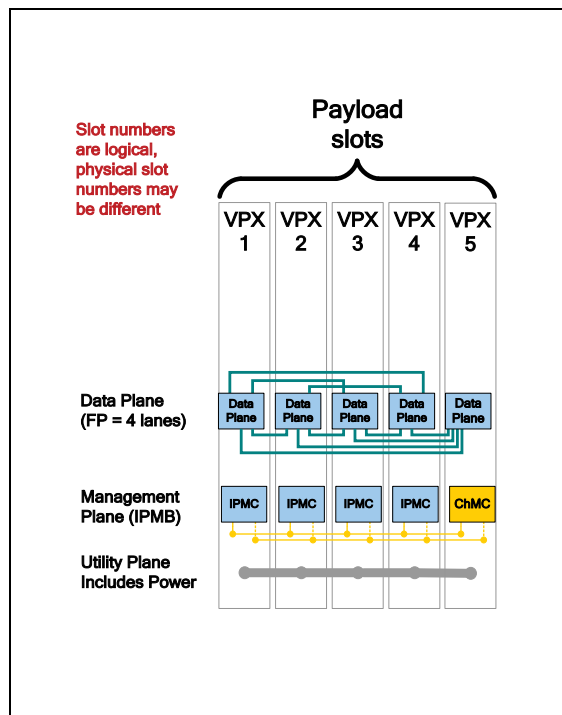
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Payload Slot Profile



SLT6-PER-4F-10.3.1

Backplane Topology



6U OpenVPX 5-Slot BKP6-DIS05-11.2.16-n Backplane

Backplane Profile

Profile name	Mechanical		Slot Profiles and Section	Channel Gbaud Rate	
	Pitch (in)	RTM Conn	Payload	Control Plane	Data Plane
BKP6-DIS05-11.2.16-1	1.0	VITA 46.10	SLT6-PER-4F -10.3.1	1.25	3.125
BKP6-DIS05-11.2.16-2	1.0	VITA 46.10	SLT6-PER-4F -10.3.1	1.25	5.0
BKP6-DIS05-11.2.16-3	1.0	VITA 46.10	SLT6-PER-4F -10.3.1	1.25	6.25

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- VPX Embedded Computing Products – SBCs, Switches, Storage, and More



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