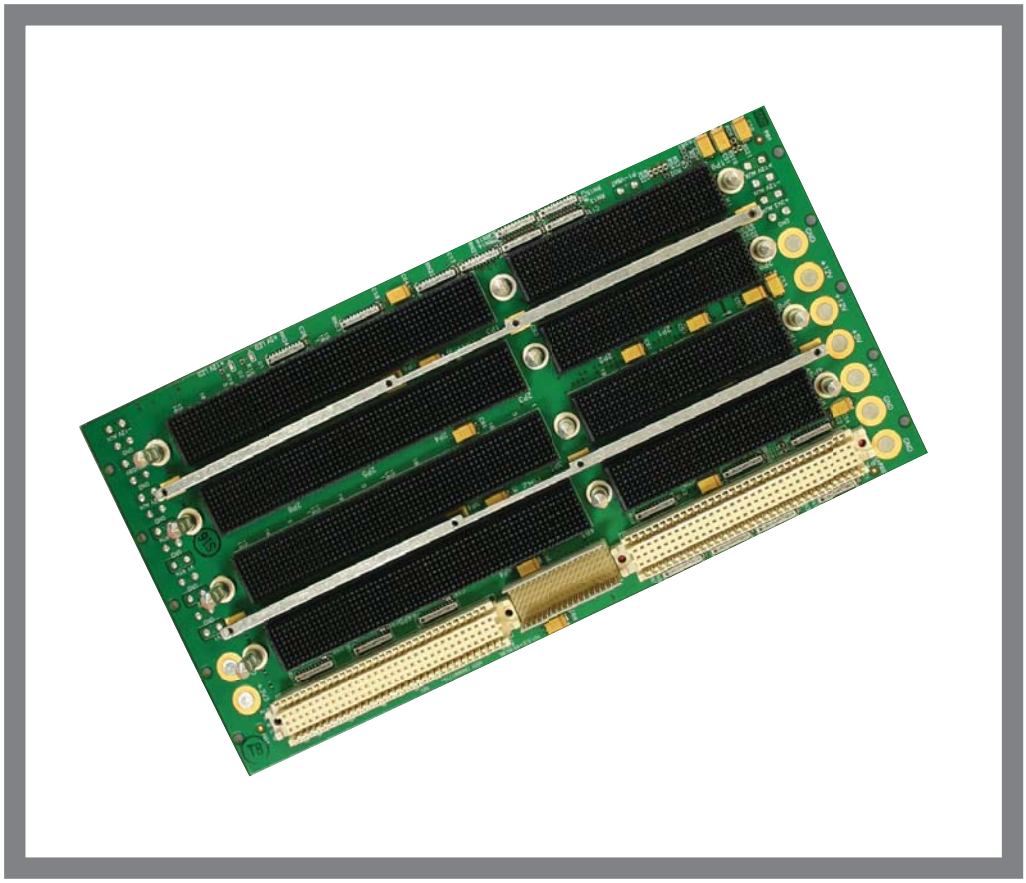
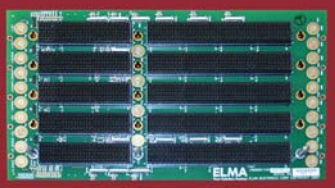
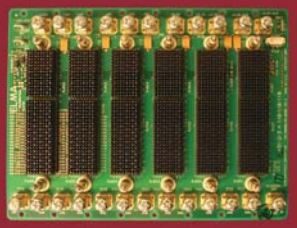
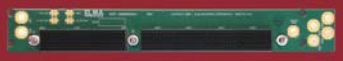
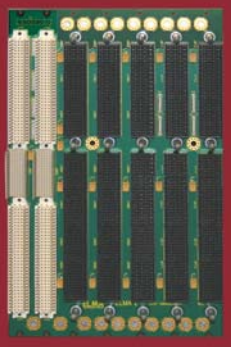










Elma Bustronic VPX
Reference Sheet

VPX
OpenVPX

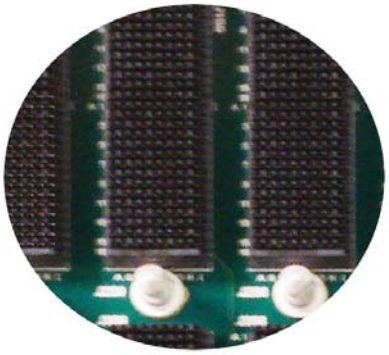
ELMA
Your Solution Partner

Rev. 1 | 11.23.09

Table of Contents

Connectors

MultiGig RT-2



Ratings	
Operating Voltage:	50 Volts AC peak or DC
Current:	1 ampere at <30/C (single circuit, free air)
Temperature:	-55 to 105/C
Low level contact resistance, circuit:	80 milliohms maximum initial 5 milliohms maximum average increase 10 milliohms maximum individual increase
Low level contact resistance, compliant pin:	1 milliohm maximum intital 1 milliohm maximum change
Insulation resistance:	1000 megohms minimum
Withstanding voltage:	1 minute hold with no breakdown or flashover
Temperature rise vs. current:	30/C maximum temperature at 1 ampere load, single circuit in free air using thermography
Mechanical	Vibration, sinusodial:
Mechanical Vibration:	No discontunuities of 1 microsecond or longer duration
Mechanical Shock:	No discontunuities of 1 microsecond or longer duration
Mating Force:	0.75 N [2.7 ozf] maximum per contact. Average for entire connector.
Unmating Force:	0.15 N [.57 ozf] minimum per contact. Average for entire connector.
Compliant pin inserton:	31 N [7 lbf] maximum per pin average
Compliant pin retention:	13.35 N [3 lbf] minimum

VME64x (160-pin DIN) - See VME Reference Sheet

Power Stud 8-32

Current Rating:	Up to 40 A @ 30 C rise
Surface Treatment:	Tin overall
Style Designator:	86 knurled shank
Head Diameter:	0.230 inches nomial
Overall length:	0.615 inches minimum and 0.635 inches maximum
Thread Length:	0.545 inches maximum nut thread
Locking Feature:	Knurled shank

Connectors

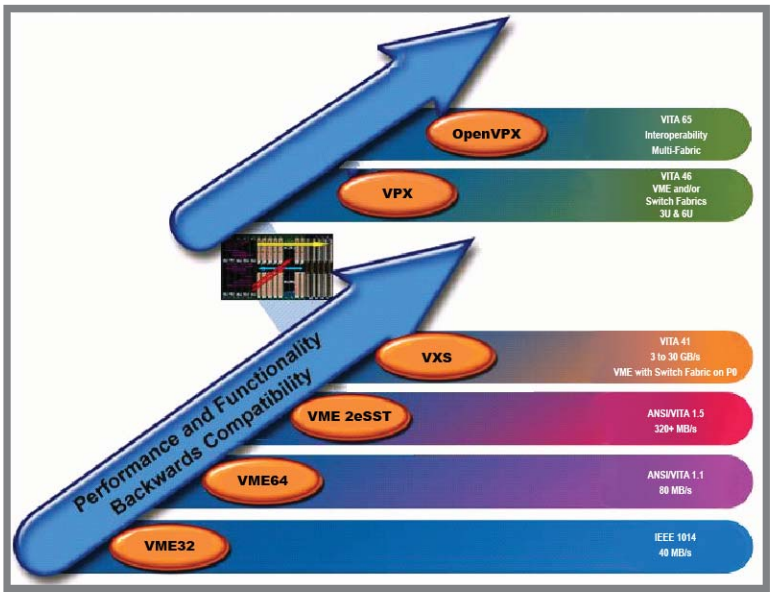
IPMB Connector (SMT)

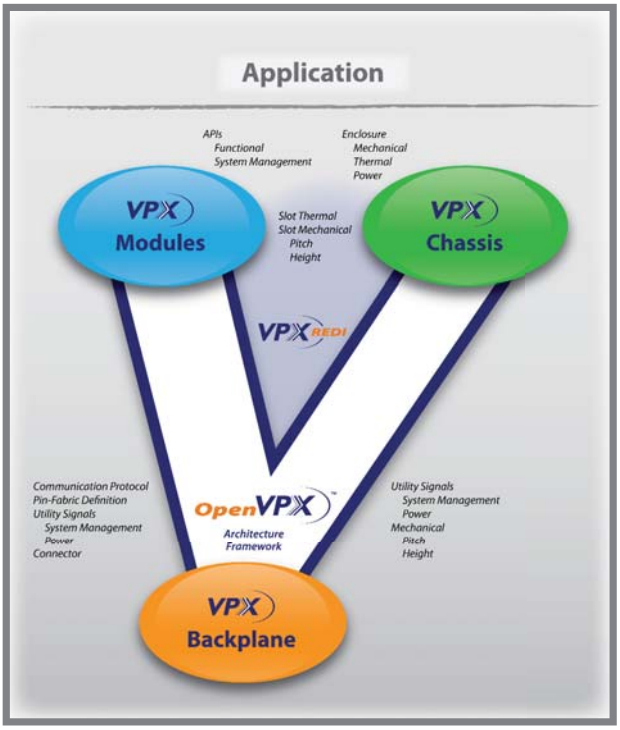
Number of Positions:	5
Number of Rows:	1
Operating Temperature:	85.0 °C (max)
Contact Material:	Phosphor Bronze
Flammability Rating:	UL 94 V-0
Gender:	Male
Housing Color:	Natural
Lead-Free Status:	Lead Free
Mounting Type:	Surface Mount
Packaging:	Tape
RoHS:	Compliant
Termination Style:	Solder Tab
Overall length:	0.615 inches minimum and 0.635 inches maximum

OpenVPX Reference Sheet

The VPX reference sheet provides relevant reference material for the VPX product line. The information provided may change at anytime. Elma Bustronic does not assume responsibility for the accuracy of the content provided within.

VME Technology Migration





OpenVPX is a process that defines system level VPX interoperability for multi-vendor, multi-module, integrated systems environment. The OpenVPX process defines clear interoperability points necessary for integration between Module to Module, Module to Backplane and Chassis. The OpenVPX V1.0 Specification, developed by VITA members, has been turned over to the VSO in October 2009 as VITA 65 for final comment, ballot, and ratification as a standard.

The OpenVPX charter is to:

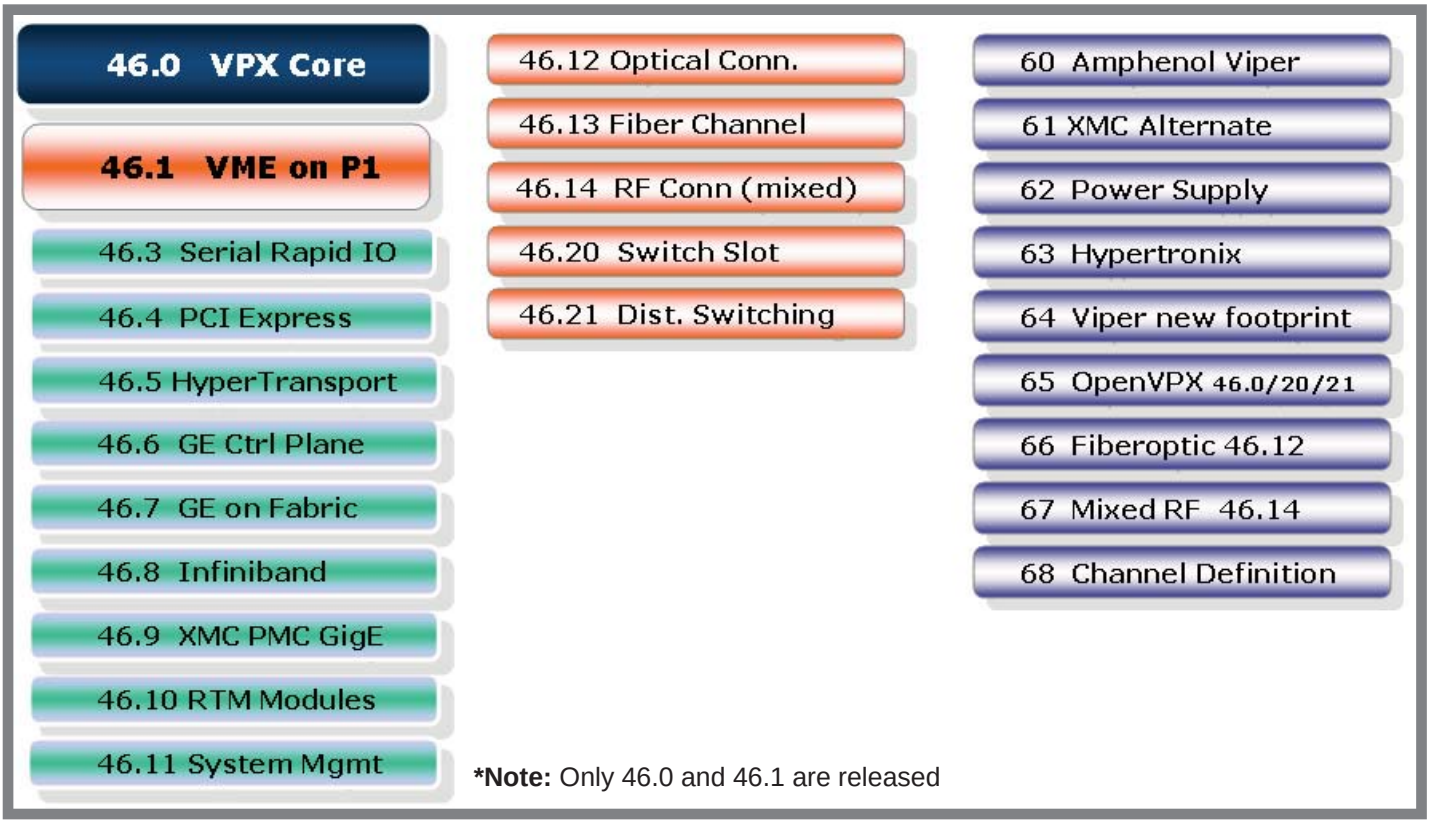
- Control and manage the assignment of VPX pins to functional planes in an interoperable architecture
- To get a high-degree of interoperability, while leaving room for sensor- / application-specific augmentation
- To make the process of developing VPX-based solutions from the lab to the field much more efficient in cost, time, quality, and repeatability

Leverage VITA

- Build upon the efforts of the VITA dot specifications
- Ensure critical functions interoperate through the development of an architecture
- Follow baseline VITA Policy and Procedures
- Submit the final work product through VITA 65 for consideration and adoption

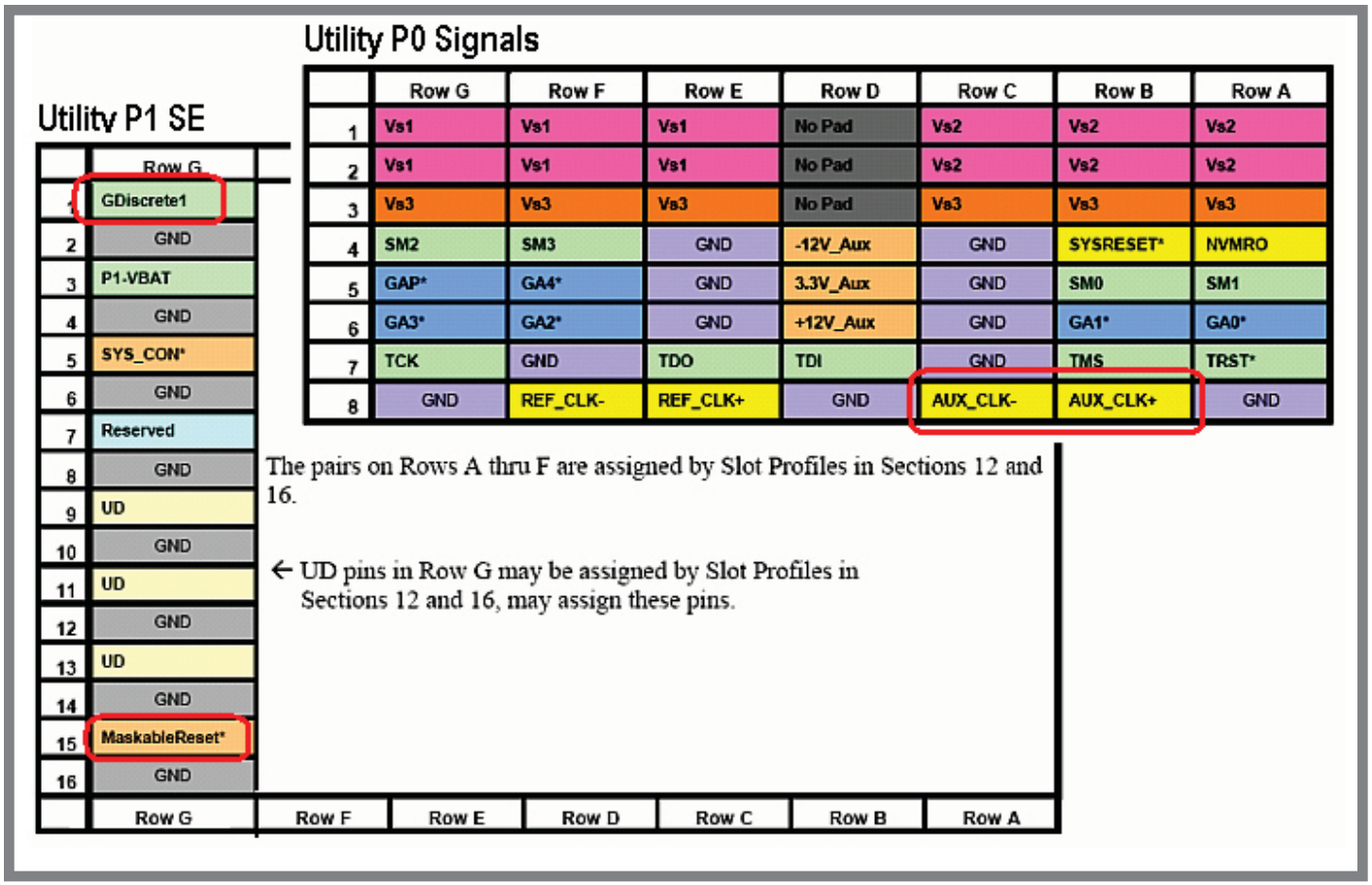
The result of the efforts was that OpenVPX provided a descriptive language for identifying module requirements and backplanes capability. It also provided with the part number configuration more information on the control and fabric planes, including the signal speeds.

VPX Standards



Utility Signal Additions

OpenVPX redefined two reserved P0/J0 signals Aux_Clk (+/-) and added one P1/J1 single ended Utility signal of Maskable Reset and redefined the Res_Bus signal to GDiscrete. The Aux_Clk and GDiscrete pins were already bussed anyway, so there is minimal effect. The SysCon signal is also now configurable.

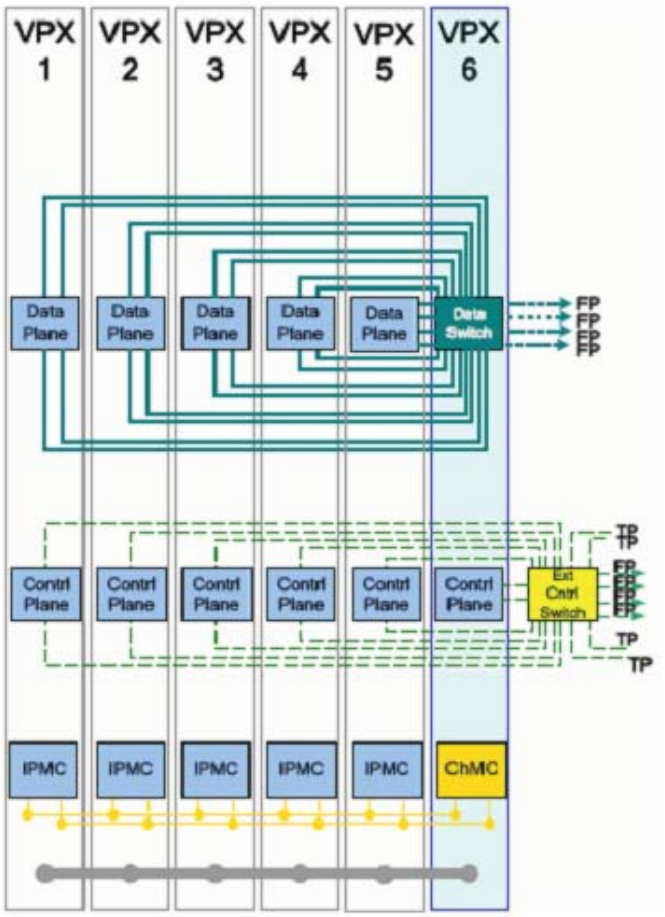


	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3
4	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1
6	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*
7	TCK	GND	TDO	TDI	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND

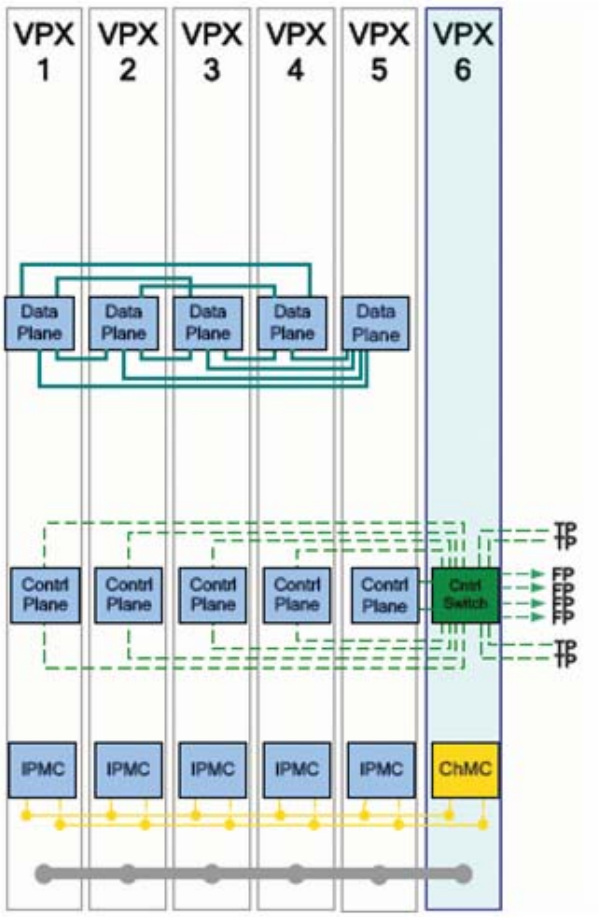
	Row G
1	GDiscrete1
2	GND
3	P1-VBAT
4	GND
5	SYS_CON*
6	GND
7	Reserved
8	GND
9	UD
10	GND
11	UD
12	GND
13	UD
14	GND
15	MaskableReset*
16	GND

Row G	Row F	Row E	Row D	Row C	Row B	Row A

Central Switched vs. Distributed Topologies



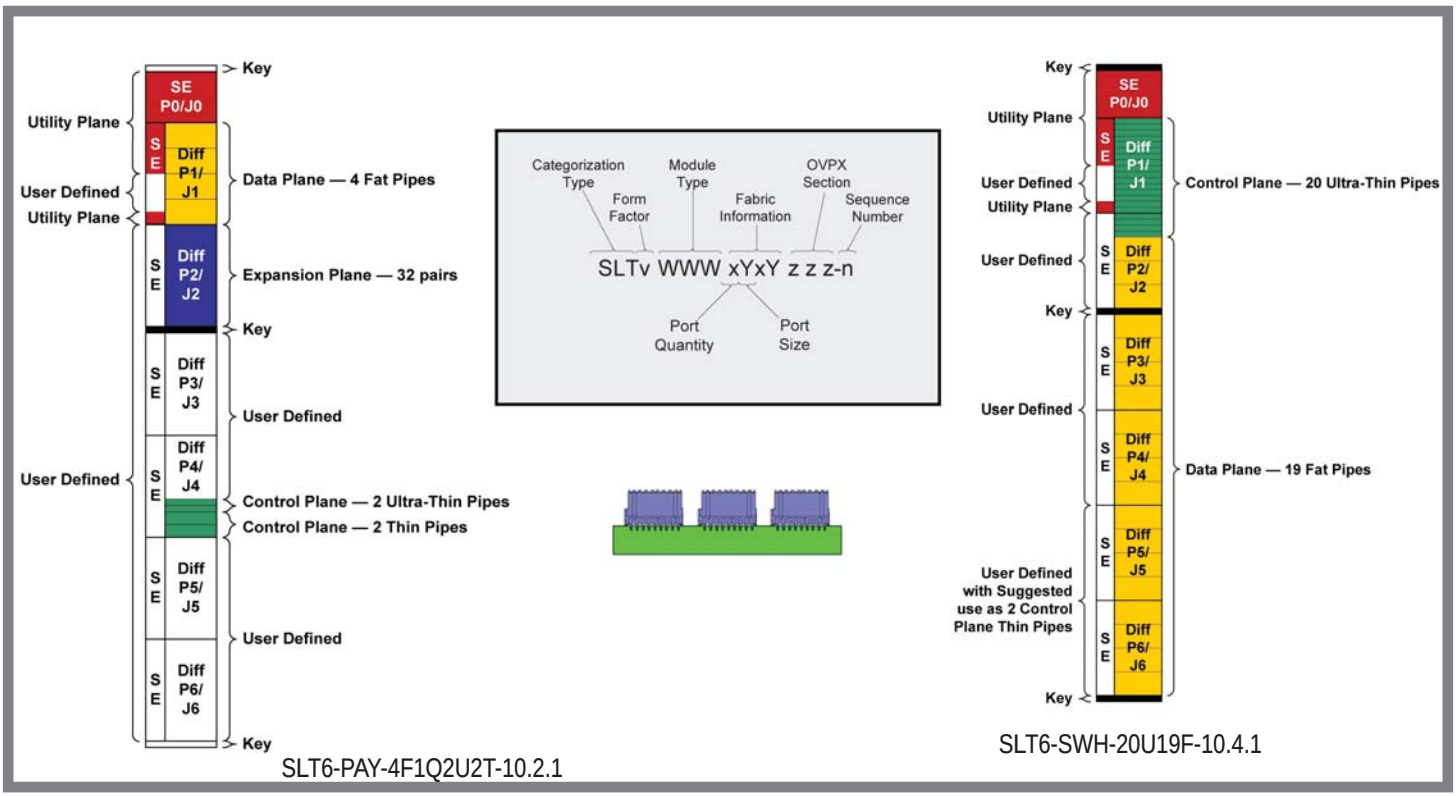
BKP6-CEN06-11.2.8-n



BKP6-DIS06-11.2.10-n

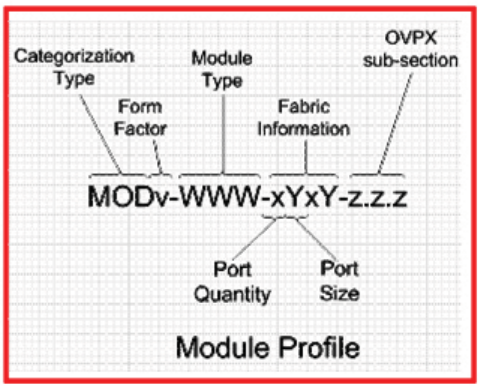
Slot Profile Examples

There are 3 types of Profiles/Configurations defined: Slot and Module Profiles, and Backplane Configurations. Each VPX module will have a specific chart of backplane signal assignments which will be registered and will define a Module Profile. Backplanes will have Slot Profiles designed to support specific VPX modules. A backplane Slot Profile may accept more than one type of Module Profile. Backplanes will be described as collections of various Slot Profiles. Backplane configurations will be further defined by how the various fabrics or planes within each Slot Profile are interconnected from slot to slot. OpenVPX modules or blades will include “peripheral” cards or “switch” cards.



Module Profile Examples

The VPX Modules and Slots across the backplanes have been given definitions so that similar Modules will work within certain Slot configurations. The backplane slot profile table describes the height, type of slot (centralized, distributed or hybrid), the pitch, RTM connector, the corresponding payload and switch cards that plug in, and the control and dataplane data rates.



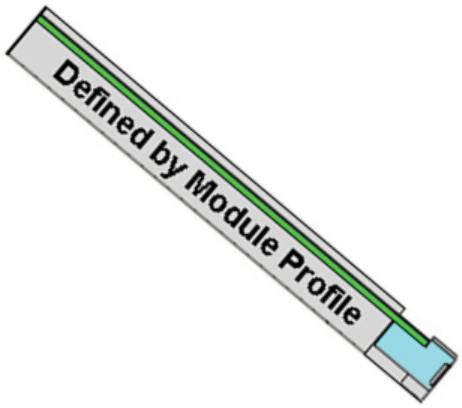


Table 12.2.2-1 Module Profiles MOD6-PAY-4F2T-12.2.2-n

Profile name	Data Plane 4 FP				Control Plane 2 TPs	
	DP01	DP02	DP03	DP04	CPtp01	CPtp02
MOD6-PAY-4F2T-12.2.2-1	SRIO 1.3 at 3.125 Gbaud per Section 5.2				1000BASE-T per Section 5.1.2	
MOD6-PAY-4F2T-12.2.2-2	PCIe Gen 1 per Section 5.3				1000BASE-T per Section 5.1.2	
MOD6-PAY-4F2T-12.2.2-3	PCIe Gen 2 per Section 5.3				1000BASE-T per Section 5.1.2	
MOD6-PAY-4F2T-12.2.2-4	10GBASE-BX4 per Section 5.1.3				1000BASE-T per Section 5.1.2	
MOD6-PAY-4F2T-12.2.2-5	10GBASE-KX4 per Section 5.1.4				1000BASE-T per Section 5.1.2	
MOD6-PAY-4F2T-12.2.2-6	SRIO 2.0 at 5.0 Gbaud per Section 5.2				1000BASE-T per Section 5.1.2	
MOD6-PAY-4F2T-12.2.2-7	SRIO 2.0 at 6.25 Gbaud per Section 5.2				1000BASE-T per Section 5.1.2	
MOD6-PAY-4F2T-12.2.2-8	SRIO 2.1 at 5.0 Gbaud per Section 5.2				1000BASE-T per Section 5.1.2	
MOD6-PAY-4F2T-12.2.2-9	SRIO 2.1 at 6.25 Gbaud per Section 5.2				1000BASE-T per Section 5.1.2	

Backplane Topology Example

The backplane configuration examples show the connectivity across the backplane for various planes. This includes the routing topology across the data plane and the connections across the expansion, control, management and utility planes. They also provide an illustration of the slot types, whether payload, switch or legacy bus slots.

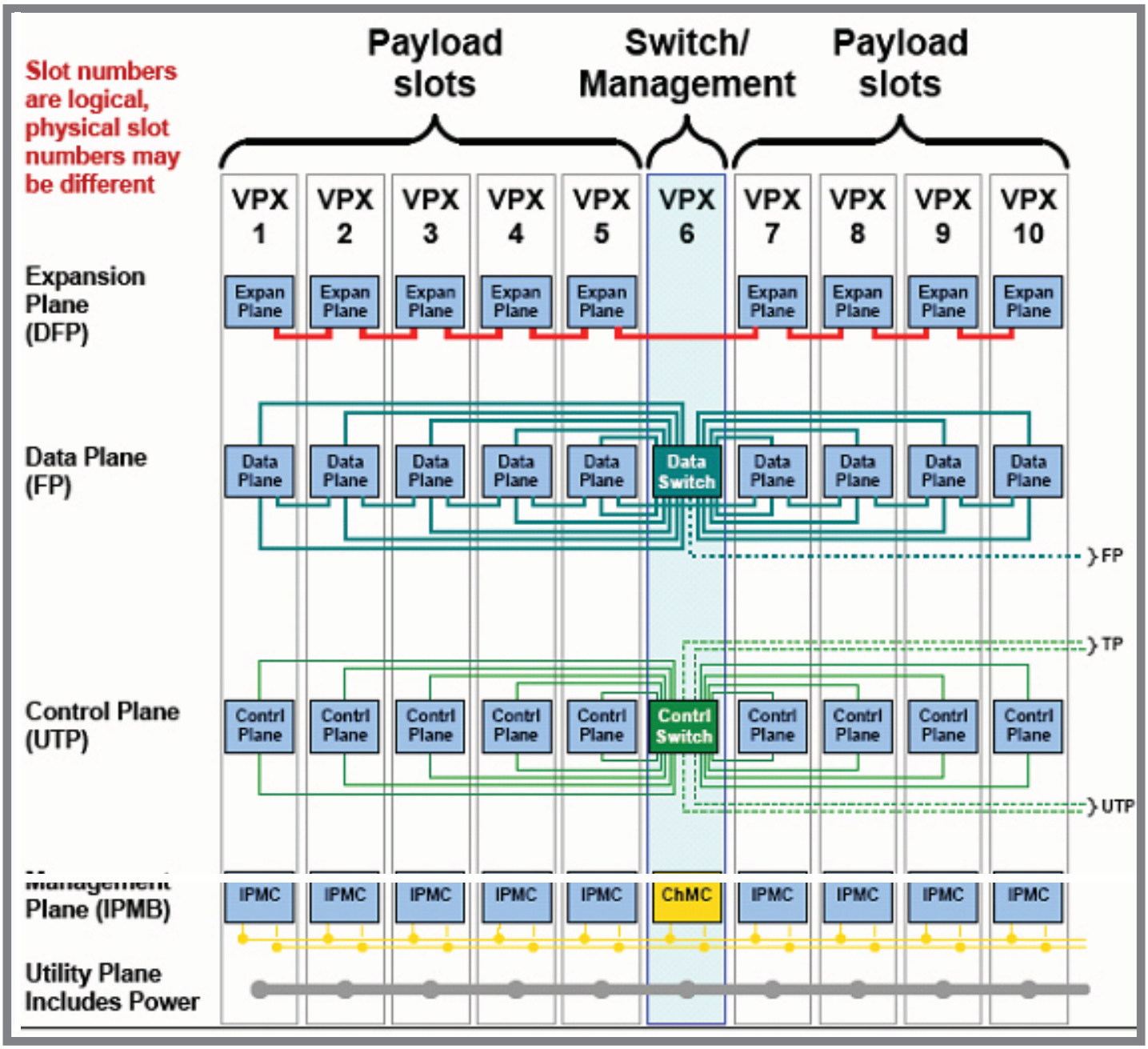


Figure 11.2.4-1 Topology of BKP6-CEN10-11.2.4-n

Wafer Design

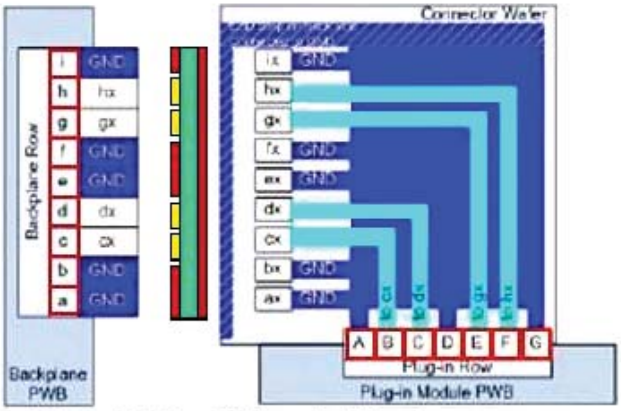


Figure 7-5: Even Differential Plug-in Module Wafer to Backplane Pin Mappings

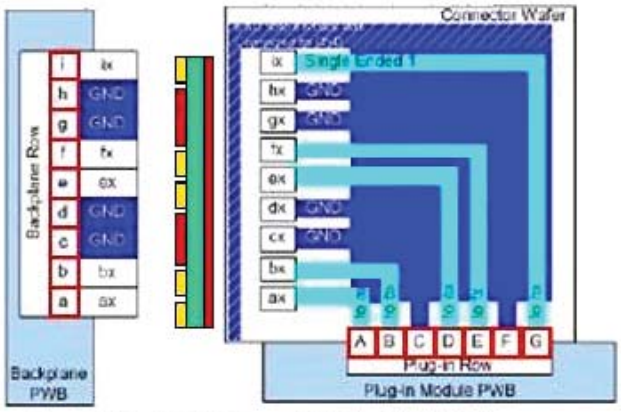
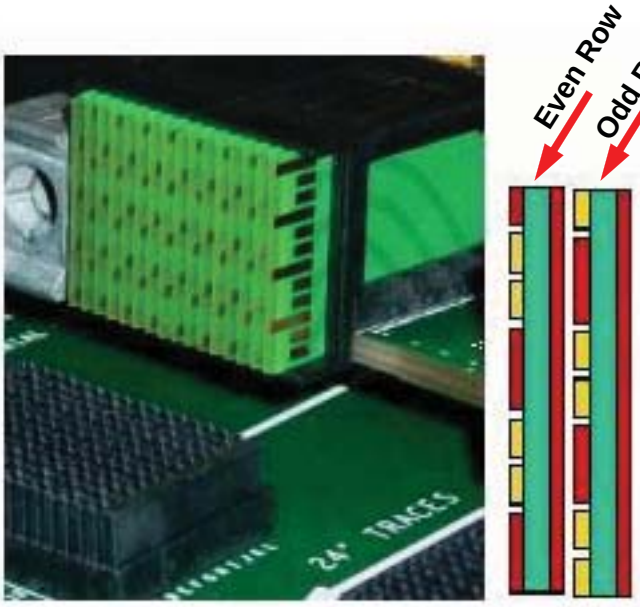


Figure 7-4: Odd Differential Plug-in Module Wafer to Backplane Pin Mappings



Note that the backplane connector signal assignments (J1-J6) are shown as having 9 rows. Note that the daughter card connector signal assignments (P1-P6) are shown as having 7 rows. Despite this fact, the two connectors really do mate properly. Why this is true, will take more graphical talent.

Backplane and Daughter Card Pinout Chart

Plug in Module P2-P6				Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Backplane J2-J6				Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	X16 using [15:0]	x8 using [7:0]	x4 using [3:0]	SEwafer1	GND	GND-J2	LN0-TD-	LN0-TD+	GND	GND-J2	LN0-RD-	LN0-RD+
2				GND	LN1-TD-	LN1-TD+	GND-J2	GND	LN1-RD-	LN1-RD+	GND-J2	GND
3				SEwafer3	GND	GND-J2	LN2-TD-	LN2-TD+	GND	GND-J2	LN2-RD-	LN2-RD+
4				GND	LN3-TD-	LN3-TD+	GND-J2	GND	LN3-RD-	LN3-RD+	GND-J2	GND
5			x4 using [7:4]	SEwafer5	GND	GND-J2	LN4-TD-	LN4-TD+	GND	GND-J2	LN4-RD-	LN4-RD+
6				GND	LN5-TD-	LN5-TD+	GND-J2	GND	LN5-RD-	LN5-RD+	GND-J2	GND
7				SEwafer7	GND	GND-J2	LN6-TD-	LN6-TD+	GND	GND-J2	LN6-RD-	LN6-RD+
8				GND	LN7-TD-	LN7-TD+	GND-J2	GND	LN7-RD-	LN7-RD+	GND-J2	GND
9		x8 using[15:8]	x4 using [11:8]	SEwafer9	GND	GND-J2	LN8-TD-	LN8-TD+	GND	GND-J2	LN8-RD-	LN8-RD+
10				GND	LN9-TD-	LN9-TD+	GND-J2	GND	LN9-RD-	LN9-RD+	GND-J2	GND
11				SEwafer11	GND	GND-J2	LN10-TD-	LN10-TD+	GND	GND-J2	LN10-RD-	LN10-RD+
12				GND	LN11-TD-	LN11-TD+	GND-J2	GND	LN11-RD-	LN11-RD+	GND-J2	GND
13			x4 using[15:12]	SEwafer13	GND	GND-J2	LN12-TD-	LN12-TD+	GND	GND-J2	LN12-RD-	LN12-RD+
14				GND	LN13-TD-	LN13-TD+	GND-J2	GND	LN13-RD-	LN13-RD+	GND-J2	GND
15				SEwafer15	GND	GND-J2	LN14-TD-	LN14-TD+	GND	GND-J2	LN14-RD-	LN14-RD+
16				GND	LN15-TD-	LN15-TD+	GND-J2	GND	LN15-RD-	LN15-RD+	GND-J2	GND

This chart shows the specifi cation pinout of both the Backplane and daughtercard for J2-J6. Note the differences between the plug-in module and the backplane (even and odd pins) for Row E and Row B. Although the number of rows is different, the connector arrangement allows single-ended signals in these areas. The backplane and daugthercard connectors mate without issue.

Higher Data Rates

Previously, VITA 46.0 defined 2.5 Gbaud* (3.125 Gbps) links

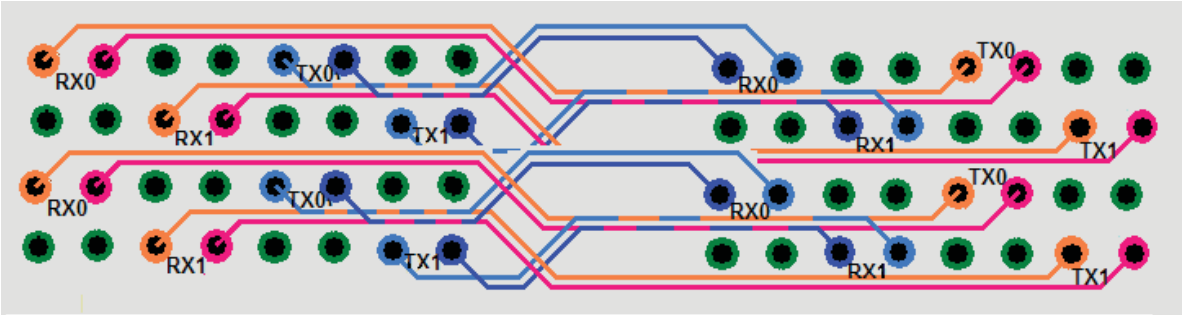
OpenVPX has added:
Data Planes at 5.0 Gbaud and 6.25 Gbaud links
Control Planes at 1 and 1.25 Gbaud per link

Profile name	Mechanical		Slot Profiles and Section		Channel Gbaud Rate		
	Pitch (in)	RTM Conn	Payload	Switch	Control Plane	Data Plane	Expan-sion Plane
BKP6-CEN10-11.2.4-1	1.0	VITA 46.10	SLT6-PAY-4F1Q2U2T-10.2.1	SLT6-SWH-20U19F-10.4.1	1.25	3.125	5.0
BKP6-CEN10-11.2.4-2	1.0	VITA 46.10	SLT6-PAY-4F1Q2U2T-10.2.1	SLT6-SWH-20U19F-10.4.1	1.25	5.0	5.0
BKP6-CEN10-11.2.4-3	1.0	VITA 46.10	SLT6-PAY-4F1Q2U2T-10.2.1	SLT6-SWH-20U19F-10.4.1	1.25	6.25	5.0

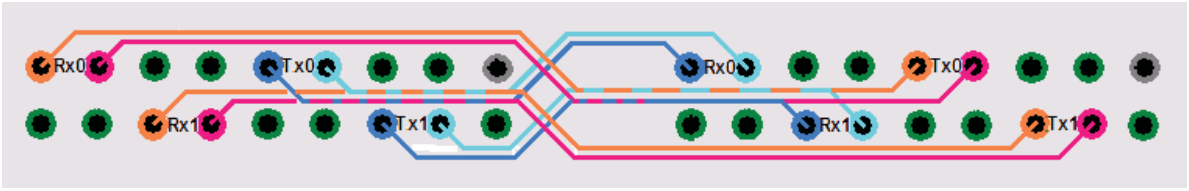
Gbaud refers to the useful data transmitted per second. Gbps is usually larger and includes additional necessary signals such as parity bits, and packet headers that are required overhead.

Channels: Fat, Thin, Ultra Thin

Fat Pipe: A channel that is comprised of four links (4 Tx pairs + 4 Rx pairs) is now being referred to as a fat pipe or by use of the x4 nomenclature. 10Gbps capable 10GBase-KX4, 10GBase-BX4, 10GBase-T, PCIe-x4, sRIO-x4, Infiniband-x4



Thin Pipe: A channel that is comprised of two links (2 Tx pairs + 2 Rx pairs) is now being referred to as a thin pipe or by use of the x2 nomenclature. 5Gbps capable 10/100/1000Base-T, 1000Base-BX, PCIe-x2, sRIO-x2, Infiniband-x2



Ultra-thin Pipe: A channel that is comprised of one link (1 Tx pair + 1 Rx pair) is now being referred to as an ultra-thin pipe or by use of the x1 nomenclature. 10GBase-KR, IGBase-KX, PCIe-x1, sRIO-x1, Infiniband-x1a

Table 2 - Various possible RTM I/O Cable Connectors

Contacts Possible within Useable 6U x 5HP Front Panel					
Connector	Length	contacts	pairs	8.45 useable	total
Stacked SCSI	42.7 / 1.68	136	68	5+	680
Airborn	54.9 / 2.16”	100	n/a	3.9	300
Infiniband	58.55 / 2.31	48	24	3.6	144
CP-50	71.2 / 2.8”	96 (144)	48	3.0	432
1x4 RJ45	59.1 / 2.36”	8	4	3.5	28(14conn)