

Features

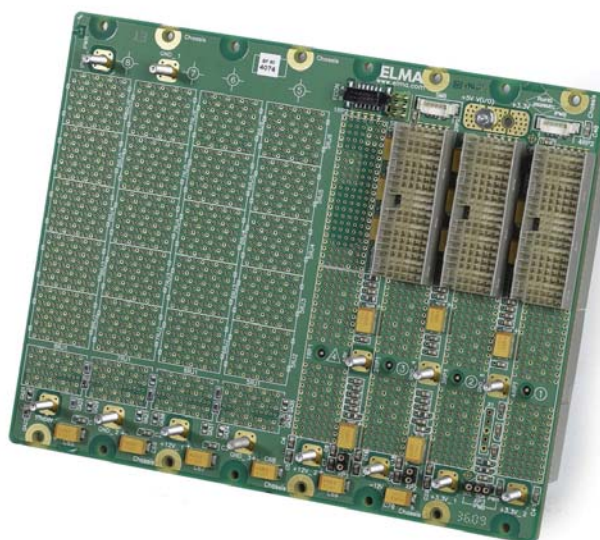
- PICMG 2.30 compliant backplane
- Hybrid function by having standard CPCI Standard Slots and CPCI – S.0 Peripheral Slots (see Pinouts chapter of this datasheet)
- High-speed connectors in the 4 x CPCI S.0 Peripheral Slots, legacy cPCI in other 4 slots
- Eurocard form factor in 3U height
- Designed to support Rear Transition Modules
- System management interface on the backplane

Board Specifications

- 12-layers
- Slot Pitch 0.8"
- PCB FR-4 or equivalent

Mechanical Specifications

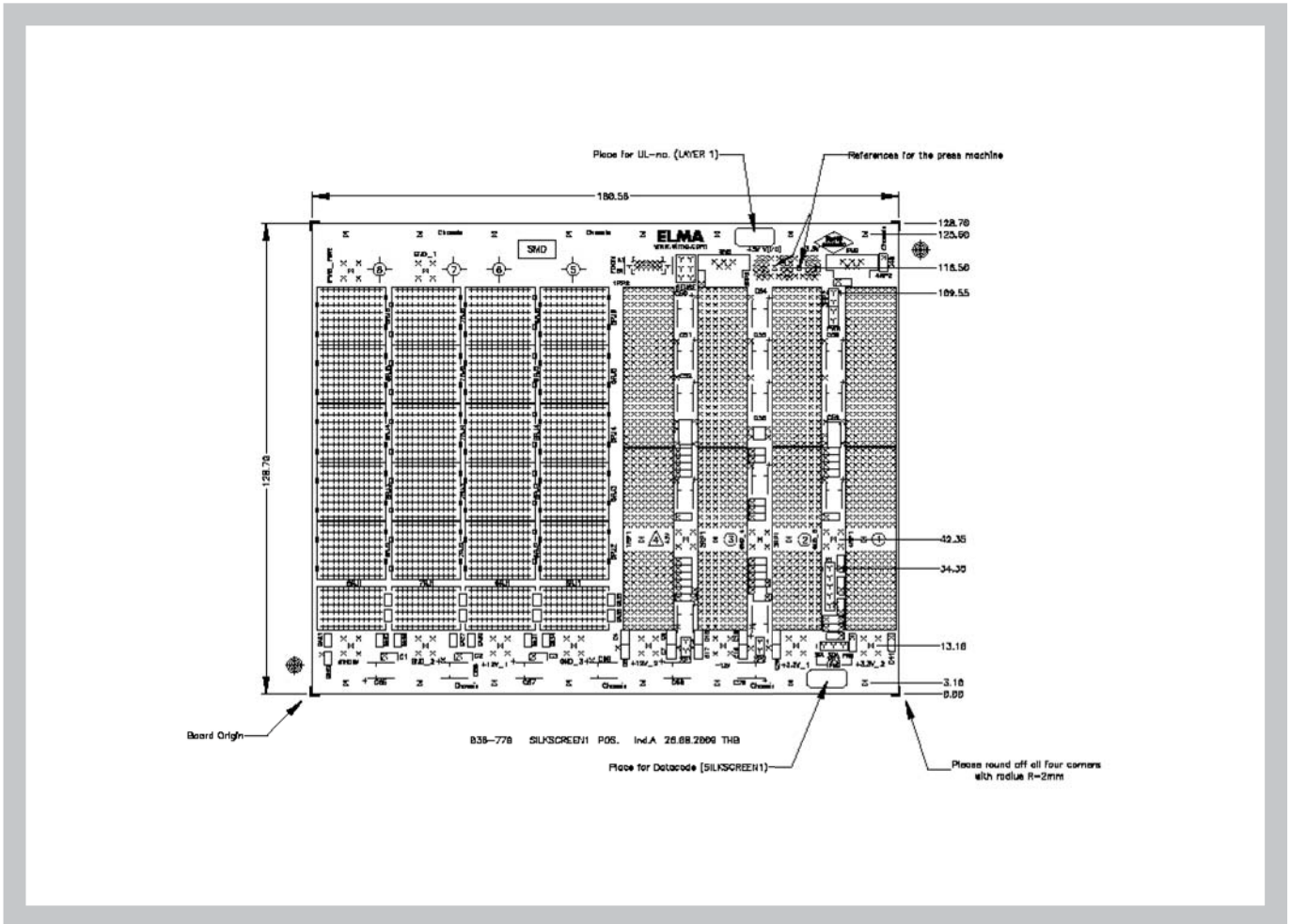
- 3U height
- 4 - slots
- PCB 160.53mm x 128.7mm
- PCB thickness 4.3mm



Rear View

CompactPCI Plus IO Backplane

Line Drawing



ORDER INFORMATION

Slots	Height	Width	Thickness	Part Number
4	3U	160.56mm	4.3mm	Consult Factory

CompactPCI Plus IO Backplane

Backplane Pinout - System Slot (CPU) Backplane

- The PICMG 2.30 System Slot acts as a Standard 32 bit CPCI System Slot
- The IO pins of the 32bit System Slot are used by PICMG 2.30 (CompactPCI PlusIO) for generating:
 - 4 x PCIe ports which are configured on this backplane as "Ultra Thin Pipe" routed in a Star Topology to the 4 x Peripheral CPCI S.0 Slots
 - 4 x USB2 ports routed in a Star Topology to the 4 x Peripheral CPCI S.0 Slots
 - 4x SATA ports routed in a Star Topology to the 4 x Peripheral CPCI S.0 Slots
 - 2 x ETHERNET ports routed in a Star Topology to the 4 x Peripheral CPCI S.0 Slots.

CPCI Plus IO System Slot (PICMG 2.30) - Pinout 1P2

Pin	Z	A	B	C	D	E	F
22	GND	GA4[S1]	GA3[S1]	GA2[S1]	GA1[S1]	GA0[S1]	GND
21	GND	CLK6	GND	2_ETH_B+	1_ETH_D+	1_ETH_B+	GND
20	GND	CLK5	GND	2_ETH_B-	1_ETH_D-	1_ETH_B-	GND
19	GND	GND	GND	2_ETH_A+	1_ETH_C+	1_ETH_A+	GND
18	GND	2_ETH_D+	2_ETH_C+	2_ETH_A-	1_ETH_C-	1_ETH_A-	GND
17	GND	2_ETH_D-	2_ETH_C-	PRST#	REQ6#	GNT6#	GND
16	GND	4_PE_CLK-	2_PE_CLK+	DEG#	GND		GND
15	GND	4_PE_CLK+	2_PE_CLK-	FAL#	REQ5#	GNT5#	GND
14	GND	3_PE_CLK-	1_PE_CLK+	4_PE_CLKE#	SATA_SCL		GND
13	GND	3_PE_CLK+	1_PE_CLK-	3_PE_CLKE#	SATA_SDO	SATA_SL	GND
12	GND	4_PE_RX00+	1_PE_CLKE#	2_PE_CLKE#	SATA_SDI	4_SATA_RX+	GND
11	GND	4_PE_RX00-	4_PE_TX00+	4_USB2+	4_SATA_TX+	4_SATA_RX-	GND
10	GND	3_PE_RX00+	4_PE_TX00-	4_USB2-	4_SATA_TX-	3_SATA_RX+	GND
9	GND	3_PE_RX00-	3_PE_TX00+	3_USB2+	3_SATA_TX+	3_SATA_RX-	GND
8	GND	2_PE_RX00+	3_PE_TX00-	3_USB2-	3_SATA_TX-	2_SATA_RX+	GND
7	GND	2_PE_RX00-	2_PE_TX00+	2_USB2+	2_SATA_TX+	2_SATA_RX-	GND
6	GND	1_PE_RX00+	2_PE_TX00-	2_USB2-	2_SATA_TX-	1_SATA_RX+	GND
5	GND	1_PE_RX00-	1_PE_TX00+	1_USB2+	1_SATA_TX+	1_SATA_RX-	GND
4	GND	VIO	1_PE_TX00-	1_USB2-	1_SATA_TX-		GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

- 2 x ETH.
- 4 x PCIE
- 4 x SATA
- 4 x USB

CPCI PLUS IO

System Slot

CPCI 2.0 R 3.0

Legacy System Slot
Δ

SLOT 4

CompactPCI Plus IO Backplane

Backplane Pinout - cPCI Serial (PIGMG cPCI - S.0) Peripheral Slots

- The Pinout of the CompactPCI Serial Slots is compliant with a very early pinout version of the PIGMG CPCI – S.0 Specification (Draft 0.6 – August 2009). For a detailed Pinout see the Pinouts Table below
- Additional ETHERNET Interconnection between 2 x Peripheral CPCI S.0 Slots (Slot5 and Slot6)

CPCI Serial Peripheral Slot (PICMG CPCI - S.0) - Pinout 5J1												
Pin	A	B	C	D	E	F	G	H	I	J	K	L
6	GND			GND			GND			GND		
5	1_PE_RX00+	1_PE_RX00-	GND	1_PE_TX00+	1_PE_TX00-	GND			GND			GND
4	GND	1_USB2+	1_USB2-	GND	1_PE_CLK+	1_PE_CLK-	GND	1_SATA_RX+	1_SATA_RX-	GND	1_SATA_TX+	1_SATA_TX-
3			GA0[1]			GA1[1]	SATA_SDI	SATA_SDO	GA2[1]	SATA_SCL	SATA_SL	GA3[1]
2	GND	IPMB_SCL	IPMB_SDA	GND	PWR_SCL	PWR_SDA	GND	RST#	WAKE_OUT#	GND	1_PE_CLKE#	
1	IPMB_PWR	STNDBY	GND	+12V	+12V	GND	+12V	+12V	GND	+12V	+12V	GND

CPCI Serial Peripheral Slot (PICMG CPCI - S.0) - Pinout 5J6												
Pin	A	B	C	D	E	F	G	H	I	J	K	L
8	GND			GND			GND			GND		
7			GND			GND			GND			GND
6	GND			GND		GND			GND			GND
5			GND			GND			GND			GND
4	GND			GND		GND			GND			GND
3			GND			GND			GND			GND
2	GND	2_ETH_AB+	2_ETH_AB-	GND	2_ETH_BA+	2_ETH_BA-	GND	2_ETH_CD+	2_ETH_CD-	GND	2_ETH_DC+	2_ETH_DC-
1	1_ETH_B+	1_ETH_B-	GND	1_ETH_A+	1_ETH_A-	GND	1_ETH_D+	1_ETH_D-	GND	1_ETH_C+	1_ETH_C-	GND

CPCI Serial Peripheral Slot (PICMG CPCI - S.0) - Pinout 6J1												
Pin	A	B	C	D	E	F	G	H	I	J	K	L
6	GND			GND			GND			GND		
5	3_PE_RX00+	3_PE_RX00-	GND	3_PE_TX00+	3_PE_TX00-	GND			GND			GND
4	GND	2_USB2+	2_USB2-	GND	2_PE_CLK+	2_PE_CLK-	GND	2_SATA_RX+	2_SATA_RX-	GND	2_SATA_TX+	2_SATA_TX-
3			GA0[2]			GA1[2]	SATA_SDI	SATA_SDO	GA2[2]	SATA_SCL	SATA_SL	GA3[2]
2	GND	IPMB_SCL	IPMB_SDA	GND	PWR_SCL	PWR_SDA	GND	RST#	WAKE_OUT#	GND	2_PE_CLKE#	
1	IPMB_PWR	STNDBY	GND	+12V	+12V	GND	+12V	+12V	GND	+12V	+12V	GND

CPCI Serial Peripheral Slot (PICMG CPCI - S.0) - Pinout 6J6												
Pin	A	B	C	D	E	F	G	H	I	J	K	L
8	GND			GND			GND			GND		
7			GND			GND			GND			GND
6	GND			GND		GND			GND			GND
5			GND			GND			GND			GND
4	GND			GND		GND			GND			GND
3			GND			GND			GND			GND
2	GND	2_ETH_BA+	2_ETH_BA-	GND	2_ETH_AB+	2_ETH_AB-	GND	2_ETH_DC+	2_ETH_DC-	GND	2_ETH_CD+	2_ETH_CD-
1	2_ETH_B+	2_ETH_B-	GND	2_ETH_A+	2_ETH_A-	GND	2_ETH_D+	2_ETH_D-	GND	2_ETH_C+	2_ETH_C-	GND

CPCI Serial Peripheral Slot (PICMG CPCI - S.0) - Pinout 7J1												
Pin	A	B	C	D	E	F	G	H	I	J	K	L
6	GND			GND			GND			GND		
5	2_PE_RX00+	2_PE_RX00-	GND	2_PE_TX00+	2_PE_TX00-	GND			GND			GND
4	GND	3_USB2+	3_USB2-	GND	3_PE_CLK+	3_PE_CLK-	GND	3_SATA_RX+	3_SATA_RX-	GND	3_SATA_TX+	3_SATA_TX-
3			GA0[3]			GA1[3]	SATA_SDI	SATA_SDO	GA2[3]	SATA_SCL	SATA_SL	GA3[3]
2	GND	IPMB_SCL	IPMB_SDA	GND	PWR_SCL	PWR_SDA	GND	RST#	WAKE_OUT#	GND	3_PE_CLKE#	
1	IPMB_PWR	STNDBY	GND	+12V	+12V	GND	+12V	+12V	GND	+12V	+12V	GND

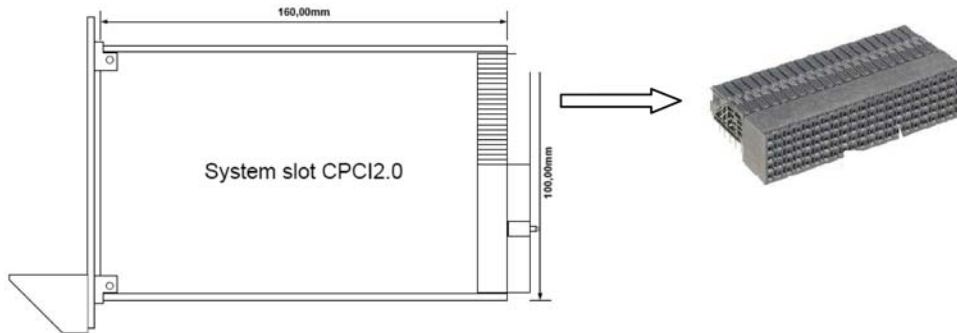
CPCI Serial Peripheral Slot (PICMG CPCI - S.0) - Pinout 8J1												
Pin	A	B	C	D	E	F	G	H	I	J	K	L
6	GND			GND			GND			GND		
5	4_PE_RX00+	4_PE_RX00-	GND	4_PE_TX00+	4_PE_TX00-	GND			GND			GND
4	GND	4_USB2+	4_USB2-	GND	4_PE_CLK+	4_PE_CLK-	GND	4_SATA_RX+	4_SATA_RX-	GND	4_SATA_TX+	4_SATA_TX-
3			GA0[4]			GA1[4]	SATA_SDI	SATA_SDO	GA2[4]	SATA_SCL	SATA_SL	GA3[4]
2	GND	IPMB_SCL	IPMB_SDA	GND	PWR_SCL	PWR_SDA	GND	RST#	WAKE_OUT#	GND	4_PE_CLKE#	
1	IPMB_PWR	STNDBY	GND	+12V	+12V	GND	+12V	+12V	GND	+12V	+12V	GND

CompactPCI Plus IO Backplane

New Backplane and Card Connectors

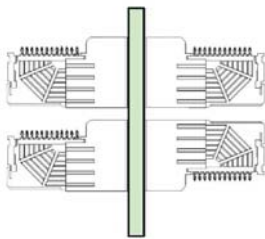
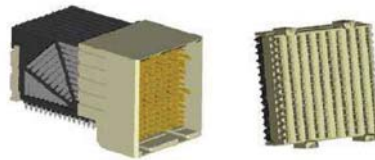
The PICMG 2.30 (CompactPCI Plus IO) CPU Board defines a new J2 connector:

- Supporting differential signals up to 5Gb/s
- Each pin is individually shielded
- Is fully compatible with the standard CPCI HM Backplane Connector



The CPCI S.0 (CompactPCI Serial) specification defines high-speed connectors:

- Supporting 12Gb/s and offering 184 pin pairs / 3U slot
- Very robust and dedicated for use also in harsh environments
- The card connector is walled on four sides
- Rear I/O using the same front side connectors



STANDARD

4 pair connector with 6 rows and 4 walls (pin guard)

ENCODING

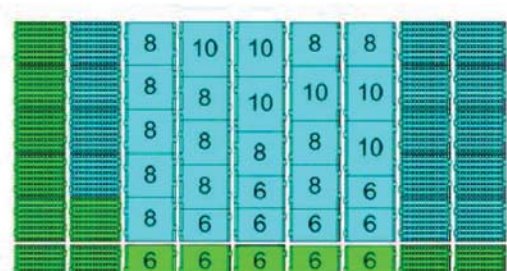
More plug and receptacle for other eventualities (coding)

4 pair connector with

- 6 rows and 2 walls
- 10 rows and 2 walls

4 pair receptacle with

- 10 rows



CompactPCI Plus IO Backplane

Additional Backplane Information

- Power studs: M3 type
- Main power input current capability:

+12V	60Amp
+5V	30Amp
+3.3V	60Amp
-12V	30Amp

Auxiliary voltages:

- STNDBY
- IPMB_PWR

System management connection : IPMB and SMB busses are routed to two 5-pin System Management bus extension connectors on the backplane, according to the PICMG 2.9 (System Management Specification):

IPMB

	Signal
1	IPMB_SCL
2	GND
3	IPMB_SDA
4	IPMB_PWR
5	ALERT#

SMB

	Signal
1	SMB_SCL
2	GND
3	SMB_SDA
4	IPMB_PWR
5	ALERT#

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