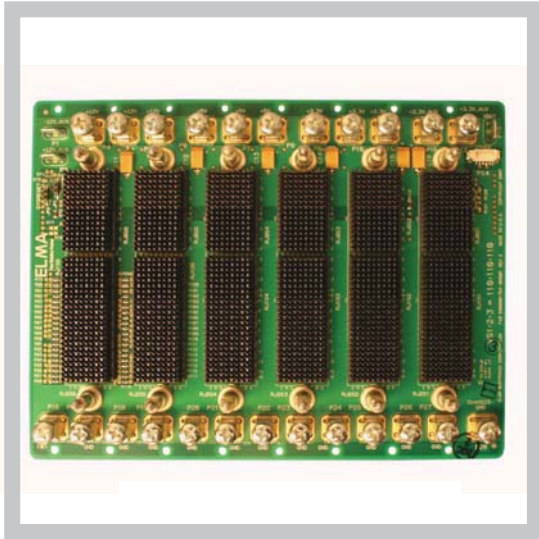


3U VPX BACKPLANES



FEATURES

- Compliant to the latest VITA 46 Specifications
- High-speed Multi-gig connector
- Uses the rugged 3U-160 Eurocard form factor
- Twisted Ring routing topology
- Switch slot for centralized switching per VITA 46.20
- All slots conform to VITA 46.3 for Serial RapidIO™ with channels A and B arranged as 2 fat pipes (x4) channels configured as a twisted ring extending from slots 1 to 5
- Provides built in ESD ground protection in every slot
- RoHS compliant versions optional
- 6U versions also available

BOARD SPECIFICATIONS

- 12-layer stripline design
- 2 oz. power and ground
- PCB FR-4 or equivalent
- PCB .145" thick

MECHANICAL SPECIFICATIONS

- 3U height
- 6-Slots
- MultiGig RT-2 connectors

DESCRIPTION

VITA 46.0 is the core document for VPX and applies to all of the subsidiary documents. Therefore because our backplanes meet the requirements of VITA 46.0 they are designed to support all of the subsidiary documents for sRIO, PCI Express, Ethernet or Infiniband. Note that VITA 46.1 and 46.20 specify additional signals that are not present in a backplane unless specifically mentioned in its description.

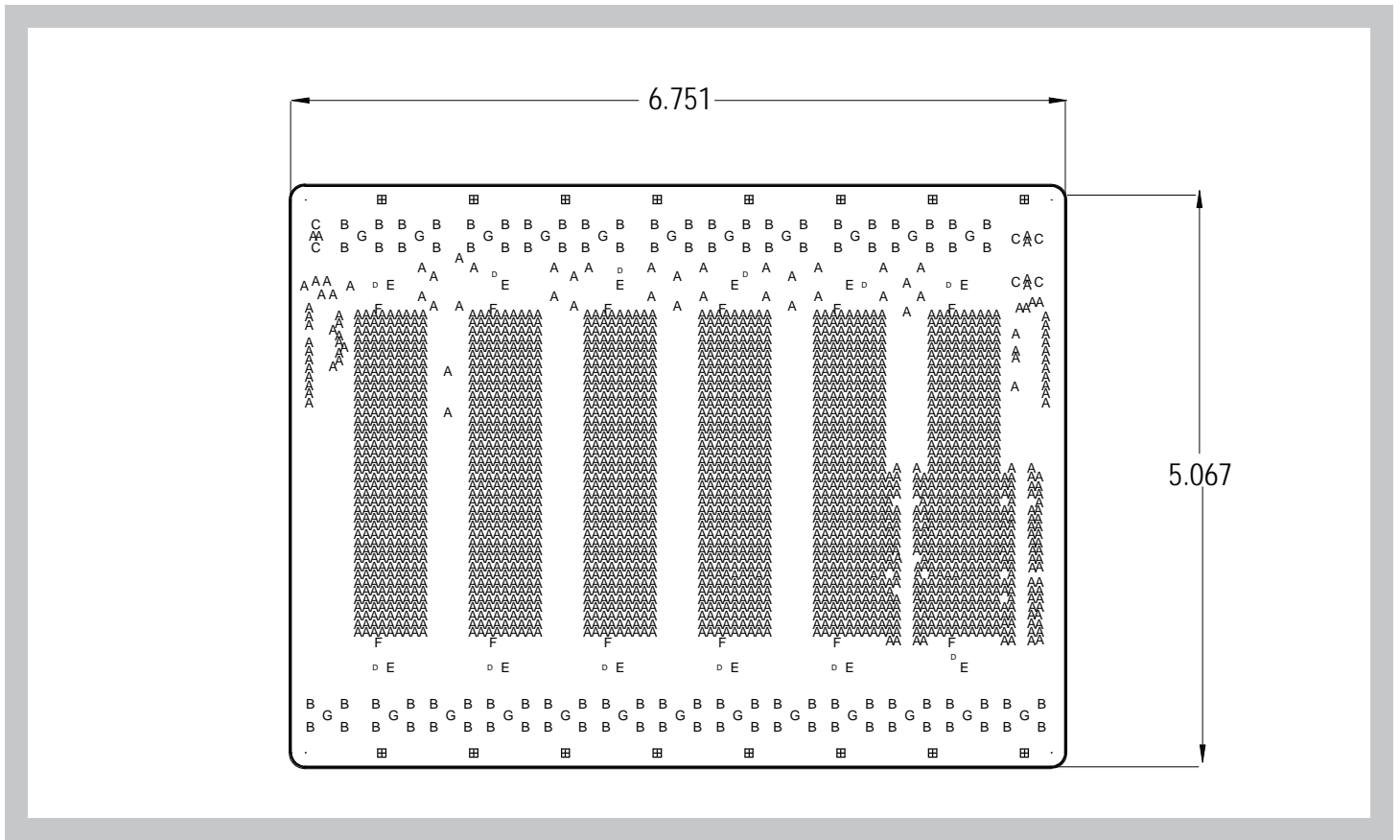
A typical 3U VPX backplane offers much less potential I/O channels than 6U VPX. However, steps have been taken to ensure the architecture offers enough flexibility and functionality. Utilizing a twisted-ring topology versus a mesh topology allows for more I/O pins and ability to use mezzanines like XMC. A full mesh topology over 3U VPX would simply take up the vast majority of available pins. In the Bustronic 3U VPX backplane to 46.20 specifications, slot 6 has configurable thin pipe links for distributed Gigabit Ethernet to slot 1 through slot 5 and two fat pipes for rear I/O. In slots 1-5 any or all of the P1 thin pipes (x2 channels) assigned to the 46.20 control channel star can be reconfigured as rear I/O by removing zero ohm SMT shunts. In slots 1-5 all P2 differential pairs are available on the rear side for I/O.

The most common configuration for 3U VPX cards is two 10-Gigabit channels at the top of the J1 connector. The remaining channels in J1 together with those in the J2 leave 24 XAUI capable bi-directional ports that can be utilized entirely for rear panel I/O. Traditionally, a channel comprised of one or two bi-directional links is referred to as a "thin pipe." A channel comprised of four bi-directional links is referred to as a "fat pipe." The 24 thin pipe channels remaining can be used by a PMC or XMC mezzanine or simply allow the 3U VPX modules to interface with external equipment, networks, displays or storage systems.

The VPX Gigabit Ethernet Control Plane per VITA 46.20 adds a GigE switch, providing a separate star or dual star network for out-of-band communication. This can be particularly important for system management, software and firmware upgrades, and initiating new processes on specific boards.

3U VPX BACKPLANES

LINE DRAWING

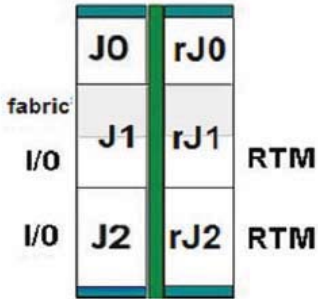


ORDER INFORMATION

Height	Total Slots	Description	Part Number
3U	6	6 slot VPX twisted ring with configurable Ethernet per VPX 46.20	101VPX306S-1X51R

3U VPX BACKPLANES

CONNECTOR POSITIONS



J0 SIGNAL ASSIGNMENTS

	Wafer Type	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Power	Vs1	Vs1	Vs1	Vs1	none	Vs2	Vs2	Vs2	Vs2
2	Power	Vs1	Vs1	Vs1	Vs1	none	Vs2	Vs2	Vs2	Vs2
3	Power	Vs3	Vs3	Vs3	Vs3	none	Vs3	Vs3	Vs3	Vs3
4	Single Ended	GND	SM2	SM3	GND	-12V_AUX	GND	SYSRESET	NMMRO	GND
5	Single Ended	GND	GAP*	GA4*	GND	3.3V_AUX	GND	SM0	SM1	GND
6	Single Ended	GND	GA3*	GA2*	GND	+12V_AUX	GND	GA1*	GA0*	GND
7	ODD DIFF	TCK	GND	GND	TD0	TD1	GND	GND	TMS	TRS T*
8	EVEN DIFF	GND	REF_CLK-	REF_CLK+	GND	GND	RES_BUS-	RES_BUS+	GND	GND

Vs1 = 12V or 48V

Vs2= 12V or 48V RTN

J1/J2 SIGNAL ASSIGNMENTS

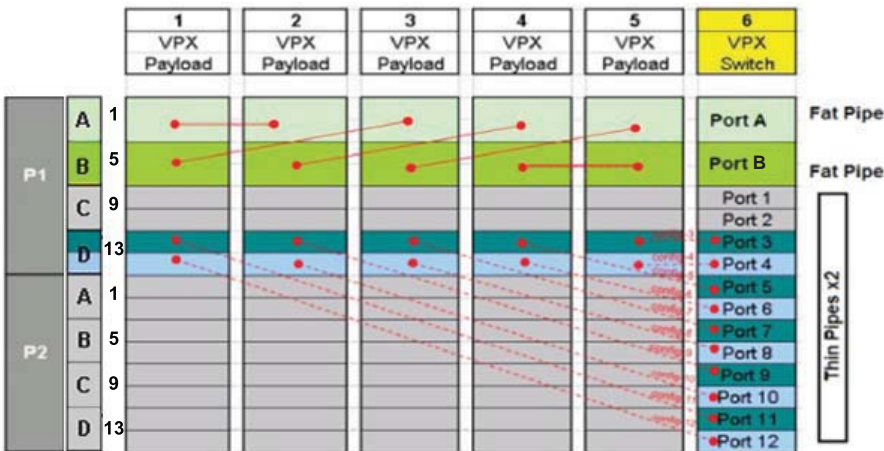
Backplane Slot J1 Connector Pin Assignments Per VITA 46.3[†] Draft 0.9

	Row A	Row B	Row C	Row D	Row E	Row F	Row G	Row H	Row I		
Channel A	1	PA-RD0+	PA-RD0-	GND	GND	PA-TD0+	PA-TD0-	GND	GND	P1*-SE0	1
	2	GND	GND	PA-RD1+	PA-RD1-	GND	GND	PA-TD1+	PA-TD1-	GND	2
	3	PA-RD2+	PA-RD2-	GND	GND	PA-TD2+	PA-TD2-	GND	GND	P1*-SE1	3
	4	GND	GND	PA-RD3+	PA-RD3-	GND	GND	PA-TD3+	PA-TD3-	GND	4
Channel B	5	PB-RD0+	PB-RD0-	GND	GND	PB-TD0+	PB-TD0-	GND	GND	P1*-SE2	5
	6	GND	GND	PB-RD1+	PB-RD1-	GND	GND	PB-TD1+	PB-TD1-	GND	6
	7	PB-RD2+	PB-RD2-	GND	GND	PB-TD2+	PB-TD2-	GND	GND	P1*-SE3	7
	8	GND	GND	PB-RD3+	PB-RD3-	GND	GND	PB-TD3+	PB-TD3-	GND	8
Channel C	9	PC-RD0+	PC-RD0-	GND	GND	PC-TD0+	PC-TD0-	GND	GND	P1*-SE4	9
	10	GND	GND	PC-RD1+	PC-RD1-	GND	GND	PC-TD1+	PC-TD1-	GND	10
	11	PC-RD2+	PC-RD2-	GND	GND	PC-TD2+	PC-TD2-	GND	GND	P1*-SE5	11
	12	GND	GND	PC-RD3+	PC-RD3-	GND	GND	PC-TD3+	PC-TD3-	GND	12
Channel D	13	PD-RD0+	PD-RD0-	GND	GND	PD-TD0+	PD-TD0-	GND	GND	P1*-SE6	13
	14	GND	GND	PD-RD1+	PD-RD1-	GND	GND	PD-TD1+	PD-TD1-	GND	14
	15	PD-RD2+	PD-RD2-	GND	GND	PD-TD2+	PD-TD2-	GND	GND	P1*-SE7	15
	16	GND	GND	PD-RD3+	PD-RD3-	GND	GND	PD-TD3+	PD-TD3-	GND	16

* This signal is P1 for connector J1, P2 for connector J2 and so on. There will be some single ended signals that are expected to be recommended by OpenVPX but these are not finalized at the present time.

† Although 46.3 is referenced this configuration of differential signals is common to VITA 46.0, 46.2, 46.3, 46.4, 46.5, 46.6...

PORT MAPPING



Ports A and B in slots 1-5 are fat pipes implemented via one twisted ring as the primary VITA 46 fabric. The fabric may be 10G Ethernet (10GBASE KX-4), sRIO, or PCIe. Slot 6 is a switch slot for a thin pipe, redundant dual star, or distributed GigE per VITA 46.20. The GigE is configurable at each of the slots 1-5 so that any individual slot could utilize ports in J1 rows 9-12 for rear I/O if desired. Port A and port B in slot 6 have 10G Ethernet rear I/O.