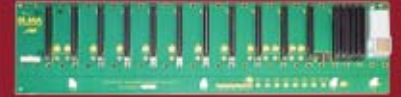


Elma Bustronic MicroTCA
User Manual



MICROTCA USER MANUAL-DUAL STAR BACKPLANE

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MICROTCA USER MANUAL-DUAL STAR BACKPLANE

MECHANICAL

Overall dimensions are 442.32mm wide by 128.9mm tall. The backplane shall not exceed 5.0mm thickness.

MICRO HUB CARRIER (MCH)

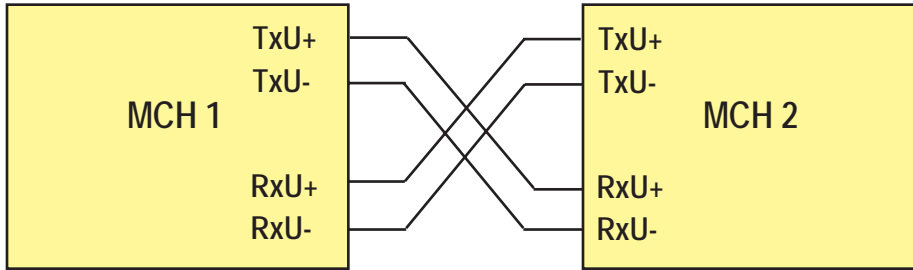
The MCH's shall be redundant. The primary MCH (MCH1) is in slot 1 and the secondary MCH (MCH2) is in slot 12.

MCH ADDRESSING:

GA [2:0]	MCMC IPMB-0 Address	MicroTCA Carrier Local Address		FRU Device ID on Carrier Manager
		Site Number	Site Type	
UUU	10h	1	MCH (0Ah)	3
PPP	12h	2	MCH (oAh)	4

MCH UPDATE MAPPING:

MCH update channel interface shall be implemented. Reference Section 6.3.1 of the MicroTCA specification. See the figure below from the MicroTCA specification for a cross-over routing diagram. All 6 update channels A, B, C, D, E, F and G will be implemented.



Update Channel A is on MCH Connector 1:

- Pin 11 TxFUA+
- Pin 12 TxFUA-
- Pin 14 RxFUA+
- Pin 15 RxFUA+

Update Channel B is on MCH Connector 2:

- Pin 8 TxFUB+
- Pin 9 TxFUB-
- Pin 162 RxFUB-
- Pin 163 RxFUB+

Update Channel D is on MCH Connector 3:

- Pin 8 TxFUD+
- Pin 9 TxFUD-
- Pin 162 RxFUD-
- Pin 163 RxFUD+

Update Channel E is on MCH Connector 3:

- Pin 11 TxFUE+
- Pin 12 TxFUE-
- Pin 159 RxFUE-
- Pin 160 RxFUE+

Update Channel F is on MCH Connector 4:

- Pin 8 TxFUF+
- Pin 9 TxFUF-
- Pin 162 RxFUF-
- Pin 163 RxFUF+

Update Channel G is on MCH Connector 4:

- Pin 11 TxFUG+
- Pin 12 TxFUG-
- Pin 159 RxFUG-
- Pin 160 RxFUG+

Update Channel G is on MCH Connector 4:

- Pin 11 TxFUG+
- Pin 12 TxFUG-
- Pin 159 RxFUG-
- Pin 160 RxFUG+

The differential impedance of the update channels lanes shall be 100 Ohms \pm 10%. Signal lengths within the differential pair should be matched to better than 3.4 ps (0.5mm in FR4 at e(r)=4.0). The transmit and receive pairs within a channel should each have a matched delay of better than 17 ps (2.54mm in FR4 at e(r)=4.0). Transmit and receive pairs may be unmatched to each other.

MICROTCA USER MANUAL-DUAL STAR BACKPLANE

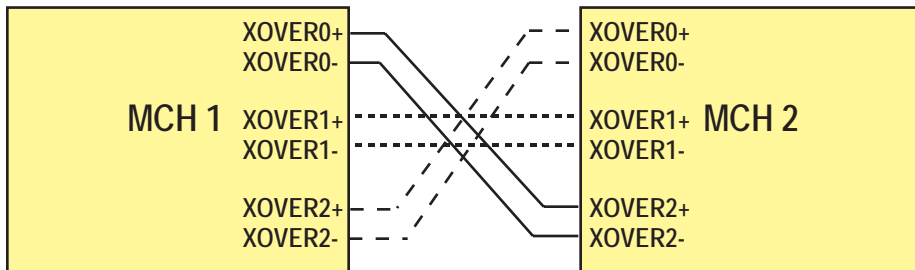
CLK 1 UPDATE CHANNEL

The CLK 1 update channel shall be implemented as below:

MCH1 Connector 2		MCH2 Connector 2	
Pin No.	Signal	Pin No.	Signal
12	CLK1_Tx-	159	CLK1_Rx-
11	CLK1_TX+	160	CLK1_Rx+
159	CLK1_Rx-	12	CLK1_Tx-
160	CLK1_Rx+	11	CLK1_Tx+

The MCH cross-over channel interface shall be implemented. Reference section 6.3.2 of the MicroTCA specification. See the below figure from the MicroTCA specification for a cross-over routing diagram.

MCH CROSS-OVER CHANNEL MAPPING



MCH 1 cross-over channel XOVER0+ shall be routed to MCH 2 cross-over channel XOVER2+. MCH 1 cross-over channel XOVER0- shall be routed to MCH 2 cross-over channel XOVER2-. MCH 1 cross-over channel XOVER2+ shall be routed to MCH 2 cross-over channel XOVER0+. MCH 1 cross-over channel XOVER2- shall be routed to MCH 2 cross-over channel XOVER0-. MCH 1 cross-over channel XOVER1+ shall be routed to MCH 2 cross-over channel XOVER1+. MCH 1 cross-over channel XOVER1- shall be routed to MCH 2 cross-over channel XOVER1-.

The cross-over channel pins are on MCH Connector 1:

- Pin 74 XOVER0+
- Pin 75 XOVER0-
- Pin 77 XOVER1+
- Pin 78 XOVER1-
- Pin 80 XOVER2+
- Pin 81 XOVER2-

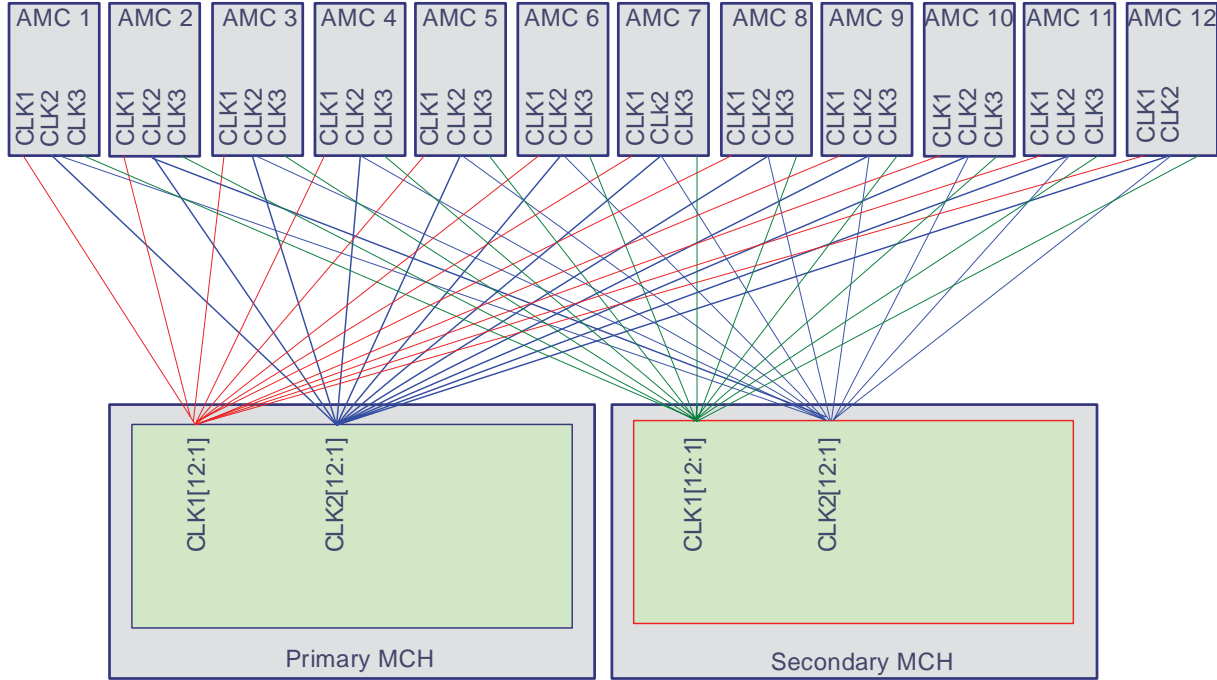
The differential impedances of the cross-over channel interface pairs shall be 100 Ohms +/- 10%.

The inter-MCH IPMB-L interface is implemented. Reference section 6.3.4 of the MicroTCA specification. MCH Connector 1 Pin 56 is SCL_L and pin 71 is SDA_L. The connection is direct: MCH 1 SCL_L to MCH 2 SCL_L and MCH 1 SDA_L to MCH 2 SDA_L.

MICROTCA USER MANUAL-DUAL STAR BACKPLANE

REDUNDANT CLOCK ARCHITECTURE

The Synchronization Clock interface will be implemented. Reference section 6.4 of the MicroTCA specification. The clocking architecture is redundant, see the figure below from the MicroTCA specification.

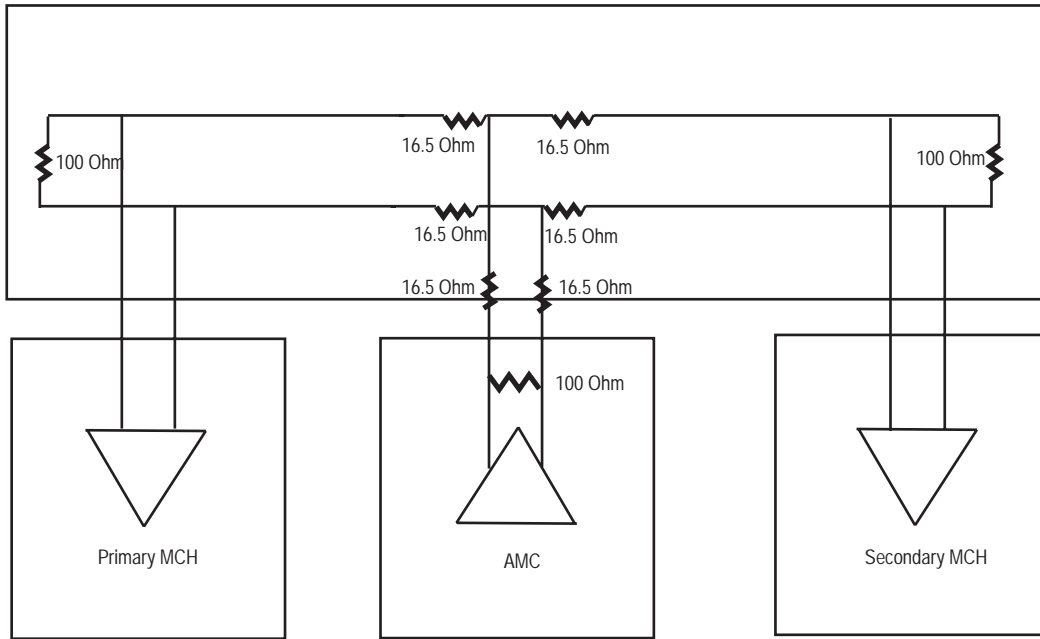


MCH Clocks 1 and 2 are implemented. The MCH 1 CLK 1 [1:10] shall be connected to AMC[1:10] (slots 2-11) CLK 1. The MCH 1 CLK 2 [1:10] shall be connected to AMC [1:10] (slots 2-11) CLK 2. The MCH 2 CLK 1 [1:10] shall be connected to AMC [1:10] (slots 2-11) CLK 3. The MCH CLK 2 [1:10] shall be connected to AMC [1:10] (slots 2-11) CLK 2.

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REDUNDANT CLOCK TERMINATION

CLK 1 shall be terminated with 100 Ohms under the MCH connectors. CLK 2 shall be terminated with 100 Ohms under the MCH connectors. CLK 1, CLK 2 and CLK 3 shall be terminated underneath each AMC connector with serial 16.5 Ohm 5% resistors to each MCH. See the figure below from the MicroTCA specification.



The trace lengths from the AMC connector to the first 16.5 Ohm resistors shall not exceed 25mm. The sum of interconnect trace lengths between the 16.5 Ohm resistors shall not exceed 10mm.

The clocks shall support M-LVDS EIA/TIA-889. Differential traces shall be length-matched to within 3.4 ps (0.5mm in FR4 at $\epsilon(r) = 4.0$) within each differential pair.

CLK1, CLK2 pin list, MCH connector 2

Pin #	Signal	Pin #	Signal
50	CLK1-1+	121	CLK2-1+
51	CLK1-1-	120	CLK2-1-
53	CLK1-2+	118	CLK2-2+
54	CLK1-2-	117	CLK2-2-
56	CLK1-3+	115	CLK2-3+
57	CLK1-3-	114	CLK2-3-
59	CLK1-4+	112	CLK2-4+
60	CLK1-4-	111	CLK2-4-
62	CLK1-5+	109	CLK2-5+
63	CLK1-5-	108	CLK2-5-
65	CLK1-6+	106	CLK2-6+
66	CLK1-6-	105	CLK2-6-
68	CLK1-7+	103	CLK2-7+
69	CLK1-7-	102	CLK2-7-
71	CLK1-8+	100	CLK2-8+
72	CLK1-8-	99	CLK2-8-
74	CLK1-9+	97	CLK2-9+
75	CLK1-9-	96	CLK2-9-
77	CLK1-10+	94	CLK2-10+
78	CLK1-10-	93	CLK2-10-

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CLK1, CLK2, CLK3, PIN LIST AMC CONNECTOR

Pin #	Signal
74	CLK1+
75	CLK1-
77	CLK2+
78	CLK2-
80	CLK3+
81	CLK3-

PLATFORM MANAGEMENT

The carrier FRU information devices are implemented as serial EEPROMs. Reference section 3.2.4 in the MicroTCA specification. The serial EEPROMs shall be Atmel AT24C256-10PI-1.8 or equivalent. One serial EEPROM connects to MCH1 via MCH connector 1 pin 129 I2C_SDA and pin 130 I2C-SCL. The other serial EEPROM connects to MCH2 via MCH connector 1 pin 129 I2C_SDA and pin 130 I2C-SCL.

IPMB-L will be implemented radically from the MCHs to the 10 AMCs using IPMBL-SDA[1:10] and IPMBL-SCL[1:10] on MCH connector 1. Reference sections 3.2.4 and 3.2.5 in the MicroTCA specification. A net list is below:

MCH Pin # and Signal Connector 1	AMC Pin # and Signal
MCH1-121 IPMBL-SCL-1	AMC1-56 SCL_L
MCH1-120 IPMBL-SDA-1	AMC1-71 SDA_L
MCH1-118 IPMBL-SCL-2	AMC2-56 SCL_L
MCH1-117 IPMBL-SDA-2	AMC2-71 SDA_L
MCH1-115 IPMBL-SCL-3	AMC3-56 SCL_L
MCH1-114 IPMBL-SDA-3	AMC3-71 SDA_L
MCH1-112 IPMBL-SCL-4	AMC4-56 SCL_L
MCH1-111 IPMBL-SDA-4	AMC4-71 SDA_L
MCH1-109 IPMBL-SCL-5	AMC5-56 SCL_L
MCH1-108 IPMBL-SDA-5	AMC5-71 SDA_L
MCH1-106 IPMBL-SCL-6	AMC6-56 SCL_L
MCH1-105 IPMBL-SDA-6	AMC6-71 SDA_L
MCH1-103 IPMBL-SCL-7	AMC7-56 SCL_L
MCH1-102 IPMBL-SDA-7	AMC7-71 SDA_L
MCH1-100 IPMBL-SCL-8	AMC8-56 SCL_L
MCH1-99 IPMBL-SDA-8	AMC8-71 SDA_L
MCH1-97 IPMBL-SCL-9	AMC9-56 SCL_L
MCH1-96 IPMBL-SDA-9	AMC9-71 SDA_L
MCH1-94 IPMBL-SCL-10	AMC10-56 SCL_L
MCH1-93 IPMBL-SDA-10	AMC10-71 SDA_L
MCH2-121 IPMBL-SCL-1	AMC1-56 SCL_L
MCH2-120 IPMBL-SDA-1	AMC1-71 SDA_L
MCH2-118 IPMBL-SCL-2	AMC2-56 SCL_L
MCH2-117 IPMBL-SDA-2	AMC2-71 SDA_L
MCH2-115 IPMBL-SCL-3	AMC3-56 SCL_L
MCH2-114 IPMBL-SDA-3	AMC3-71 SDA_L
MCH2-112 IPMBL-SCL-4	AMC4-56 SCL_L
MCH2-111 IPMBL-SDA-4	AMC4-71 SDA_L
MCH2-109 IPMBL-SCL-5	AMC5-56 SCL_L
MCH2-108 IPMBL-SDA-5	AMC5-71 SDA_L
MCH2-106 IPMBL-SCL-6	AMC6-56 SCL_L
MCH2-105 IPMBL-SDA-6	AMC6-71 SDA_L
MCH2-103 IPMBL-SCL-7	AMC7-56 SCL_L
MCH2-102 IPMBL-SDA-7	AMC7-71 SDA_L
MCH2-100 IPMBL-SCL-8	AMC8-56 SCL_L
MCH2-99 IPMBL-SDA-8	AMC8-71 SDA_L
MCH2-97 IPMBL-SCL-9	AMC9-56 SCL_L
MCH2-96 IPMBL-SDA-9	AMC9-71 SDA_L
MCH2-94 IPMBL-SCL-10	AMC10-56 SCL_L
MCH2-93 IPMBL-SDA-10	AMC10-71 SDA_L

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PLATFORM MANAGEMENT

AMC slots shall provide geographical addressing according to Table 3-5 in the MicroTCA Specification.

IPMB-0 will be implemented. Reference section 3.2.2 in the MicroTCA Specification. The IPMB0_A bus will be connected between MCH1 connector 1 IPMB0_A and power module 1 IPMB0_A and MCH2 connector 1 IPMB0_A power module 2 IPMB0_A. IPMB0_B bus will be connected between MCH1 connector 1 IPMB0_B0_B and MCH2 connector 1 IPMB0_B and power module 2 IPMB0_B. A net list is below:

MCH Connector 1		PM/Fans
Pin #	Signal	Pin # Signal
MCH1-126	IPMB0-SDA-A	PM1-F9SDA_A, PM2-F9 SDA_A, PM1-F9 SDA_A, PM2-F9 SDA_A, P1-6 IPMB0-SDA, P5-6 IPMB0-SDA
MCH1-127	IPMB0-SCL-A	PM1-E9 SCL_A, PM2-E9 SCL_A, PM1-E9 SCL_A, PM2-E9 SCL_A, P1-5 IPMB0-SCL, P5-5 IPMB0-SCL
MCH1-123	IPMB0-SDA-B	PM1-D9 SDA_B, PM2-D9 SDA_B, PM1-D9 SDA_B, PM2-D9 SDA_B, P2-6 IPMB0-SDA, P6-6 IPMB0-SDA
MCH1-124	IPMB0-SCL-B	PM1-C9 SCL_B, PM2-C9 SCL_B, PM1-C9 SCL_B, PM2-C9 SCL_B, P2-5 IPMB0-SCL, P6-5 IPMB0-SCL
MCH2-126	IPMB0-SDA-A	MCH1-126 IPMB0-SDA-A, P4-6 IPMB0-SDA, P8-6 IPMB0-SDA
MCH2-127	IPMB0-SCL-A	MCH1-127 IPMB0-SCL-A, P4-5 IPMB0-SCL, P8-5 IPMB0-SCL
MCH2-123	IPMB0-SDA-B	MCH1-123 IPMB0-SDA-B, P3-6 IPMB0-SDA, P7-6 IPMB0-SDA
MCH2-124	IPMB0-SCL-B	MCH1-124 IPMB0-SCL-B, P3-5 IPMB0-SCL, P7-5 IPMB0-SCL

POWER MODULES

The MCH and each AMC payload power channel shall be capable of carrying 9.7.A.

Power channel mapping and management power mapping should follow the table below. Refer to section 3.8.1 in the MicroTCA specification.

POWER CHANNEL MAPPING

Power Channel	Management Power	Payload Power	PS#1	ENABLE#	Autonomous Power
1-2	MP_MCH1- PP_MCH2	PP_MCH1- PP_MCH2	PS1_MCH1#- PS1_MCH2#	EN_MCH1#- EN_MCH2#	Depends on PWR_ON1- PWR_ON2
3-4	MP_CU1- MP_CU2	PP_CU1- PP_CU2	PS1_CU1#- PS1_CU2#	EN_CU1#- EN_CU2#	Yes
5-16	MP_1- MP_12	PP_1- PP_12	PS1_1#- PS1_12#	EN_1#- EN_12#	No

MICROTCA USER MANUAL-DUAL STAR BACKPLANE

POWER MODULES

PS1# will be implemented radially from each power module to each MCH and all AMCs. Refer to section 3.2.1 and 3.8.1 in the MicroTCA Specification. Note: The following netlist assumes Figure 6-14 "Redundant MicroTCA system example" on page 6-40 of the MicroTCA Specification is incorrect.

PM Pin Out		MCH/AMC Pin Out	
Pin #	Signal	Pin #	Signal
PM1-C1	PS1_M1	MCH1-3	PS1# Connector 1
PM1-C8	PS1_M2	MCH2-3	PS1# Connector 1
PM1-D2	PS1_1#	AMC1-3	PS1#
PM1-C2	PS1_2#	AMC2-3	PS1#
PM1-D3	PS1_3#	AMC3-3	PS1#
PM1-C3	PS1_4#	AMC4-3	PS1#
PM1-D4	PS1_5#	AMC5-3	PS1#
PM1-C4	PS1_6#	AMC6-3	PS1#
PM1-D5	PS1_7#	AMC7-3	PS1#
PM1-C5	PS1_8#	AMC8-3	PS1#
PM1-D6	PS1_9#	AMC9-3	PS1#
PM1-C6	PS1_10#	AMC10-3	PS1#
PM2-C2	PS1_M1	MCH1-3	PS1# Connector 1
PM2-C8	PS1_M2	MCH2-3	PS1# Connector 1
PM2-D2	PS1_1#	AMC1-2	PS1#
PM2-C2	PS1_2#	AMC2-3	PS1#
PM2-D3	PS1_3#	AMC3-3	PS1#
PM2-C3	PS1_4#	AMC4-3	PS1#
PM2-D4	PS1_5#	AMC5-3	PS1#
PM2-C4	PS1_6#	AMC6-3	PS1#
PM2-D5	PS1_7#	AMC7-3	PS1#
PM2-C5	PS1_8#	AMC8-3	PS1#
PM2-D6	PS1_9#	AMC9-3	PS1#
PM2-C6	PS1_10#	AMC10-3	PS1#

The Presence signal for the cooling units is covered in the Cooling Unit section.

MICROTCA USER MANUAL-DUAL STAR BACKPLANE

POWER MODULES

EN# will be implemented radially from each power module to each MCH and all AMCs. Refer to section 3.2.1 and 3.8.1 in the MicroTCA Specification. Note: The following netlist assumes Figure 6-14 "Redundant MicroTCA system example" on page 6-40 of the MicroTCA Specification is incorrect.

PM Pin Out		MCH/AMC Pin Out	
Pin #	Signal	Pin #	Signal
PM1-E1	EN_M1#	MCH1-41	ENABLE# Connector 1
PM1-E8	EN_M2#	MCH2-41	ENABLE# Connector 1
PM1-F2	EN_1#	AMC1-41	ENABLE#
PM1-E2	EN_2#	AMC2-41	ENABLE#
PM1-F3	EN_3#	AMC3-41	ENABLE#
PM1-E3	EN_4#	AMC4-41	ENABLE#
PM1-F4	EN_5#	AMC5-41	ENABLE#
PM1-E4	EN_6#	AMC6-41	ENABLE#
PM1-F5	EN_7#	AMC7-41	ENABLE#
PM1-E5	EN_8#	AMC8-41	ENABLE#
PM1-F6	EN_9#	AMC9-41	ENABLE#
PM1-E6	EN_10#	AMC10-41	ENABLE#
PM2-E1	EN_M1#	MCH1-41	ENABLE# Connector 1
PM2-E8	EN_M2#	MCH2-41	ENABLE# Connector 1
PM2-F2	EN_1#	AMC1-41	ENABLE#
PM2-E2	EN_2#	AMC2-41	ENABLE#
PM2-F3	EN_3#	AMC3-41	ENABLE#
PM2-E3	EN_4#	AMC4-41	ENABLE#
PM2-F4	EN_5#	AMC5-41	ENABLE#
PM2-E4	EN_6#	AMC6-41	ENABLE#
PM2-F5	EN_7#	AMC7-41	ENABLE#
PM2-E5	EN_8#	AMC8-41	ENABLE#
PM2-F6	EN_9#	AMC9-41	ENABLE#
PM2-E6	EN_10#	AMC10-41	ENABLE#

The enable signal for cooling units is covered in the Cooling Units section.

PWR_ON will be implemented, reference section 6.3.3 in the MicroTCA Specification.

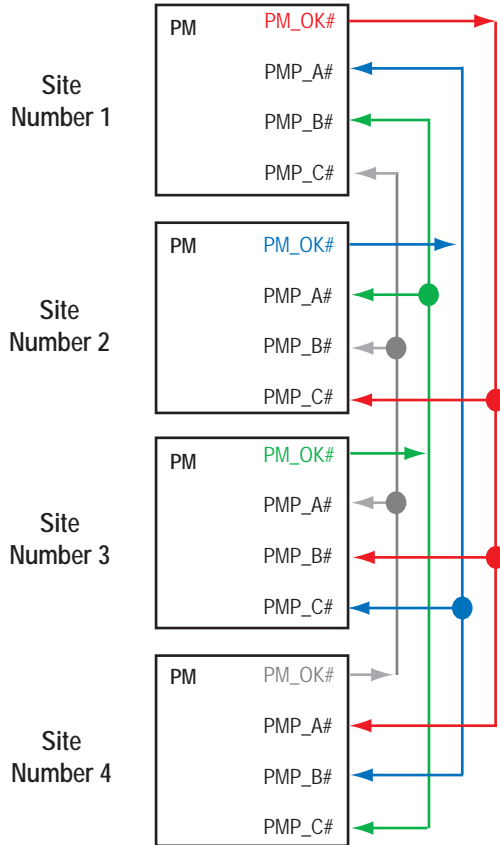
PM Pin Out		MCH Pin Out	
Pin #	Signal	Pin #	Signal
PM1-H9	PWR_ON_M1	MCH1-170	PWR_ON Connector 1
PM1-G9	PWR_ON_M2	MCH2-170	PWR_ON Connector 1
PM1-H9	PWR_ON_M1	MCH1-170	PWR_ON Connector 1
PM1-G9	PWR_ON_M2	MCH2-170	PWR_ON Connector 1

MICROTCA USER MANUAL-DUAL STAR BACKPLANE

POWER MODULES

PWR_OK# and the PMP[A:C]# signals shall be implemented per the figure below.

COMMUNICATION OF POWER MODULE PRESENCE AND POWER GOOD



See the netlist below:

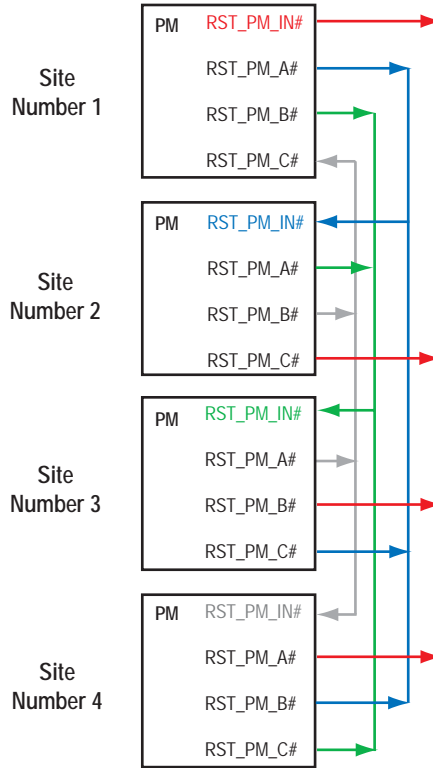
PM Pin Out	Signal	PM Pin Out	Signal
Pin #		Pin #	
PM1-B1	PM_OK#	PM2-B4	PMP_C#
PM1_B2	PMP_A#	PM2-B1	PM_OK#
PM1-B3	PMP_B#	PM2-B3	PMP_A#
PM1-B4	PMP_C#	PM2-B3	PMP_B#

MICROTCA USER MANUAL-DUAL STAR BACKPLANE

POWER MODULES

RST_PM_IN# and the RST_PM[A:C]# signals shall be implemented per the figure below.

COMMUNICATION OF PM REST SIGNALS



See the netlist below:

PM Pin Out		PM Pin Out	
Pin #	Signal	Pin #	Signal
PM1-B5	RST_PM_IN#	PM2-B8	RST_PM_C#
PM1-B6	RST_PM_A#	PM2-B5	RST_PM_IN#
PM1-B7	RST_PM_B#	PM2-B6	RST_PM_A#
PM1-B8	RST_PM_C#	PM2-B7	RST_PM_B#

PS_PM# is tied to ground.

PS0# on the MCHs, pin 83 on connector 1, and on the AMCs, pin 83 shall be connected to ground.

POWER MODULE AND COOLING UNIT ADDRESSING

Geographical addressing will be supported according to the table below.

GA[2:0]	IPMB-0 Address	MicroTCA Carrier Local Address		Carrier Manager FRU Device ID
		Site Number	Site Type	
GGU	A8h	1	Cooling Unit (04h)	40
GUG	AAh	2	Cooling Unit (04h)	41
GGU	C2h	1	Power Module (0Bh)	50
GUG	C4h	2	Power Module (0Bh)	51
GUU	C6h	3	Power Module (0Bh)	52
UGG	C8h	4	Power Module (0Bh)	53

MICROTCA USER MANUAL-DUAL STAR BACKPLANE

COOLING UNIT

Eight Cooling Unit (CU) connectors are on the backplane. The connectors shall be labeled P1-P8. The fan connector shall be Molex 53261-1071. The connectors will be labeled sequentially starting at the top right corner, proceeding to the right, then down and to the right. The pinouts are as follows:

P1 and P5:

1	PP_CU1	PM1-P2
2	GND	
3	MP_CU1	PM1-H3
4	GND	
5	IPMB0_SCL_A	MCH1-127
6	IPMB0_SDA_A	MCH1-126
7	GND	
8	PS1_CU1#	PM1-D1
9	EN_CU1#	PM1-F1
10	PP_CU1	

P2 and P6:

1	PP_CU2	PM1-P3
2	GND	
3	MP_CU2	PM1-H8
4	GND	
5	IPMB0_SCL_B	MCH1-124
6	IPMB0_SDA_B	MCH1-123
7	GND	
8	PS1_CU2#	PM1-D8
9	EN_CU2#	PM1-F8
10	PP_CU1	

P3 and P7:

1	PP_CU2	PM2-P3
2	GND	
3	MP_CU2	PM2-H8
4	GND	
5	IPMB0_SCL_B	MCH2-124
6	IPMB0_SDA_B	MCH2-123
7	GND	
8	PS1_CU2#	PM2-D8
9	EN_CU2#	PM2-F8
10	PP_CU1	

P4 and P8:

1	PP_CU1	PM2-P2
2	GND	
3	MP_CU1	PM2-H3
4	GND	
5	IPMB0_SCL_A	MCH2-127
6	IPMB0_SDA_A	MCH2-126
7	GND	
8	PS1_CU1#	PM2-D1
9	EN_CU1#	PM2-F1
10	PP_CU1	

Refer back to the platform management section for IPMB0 bussing.

MICROTCA USER MANUAL-DUAL STAR BACKPLANE

FABRIC INTERFACE

MCH Fabric [A] is routed to AMC Port [0] on each slot. See below for a netlist. Reference section 6.2 in the MicroTCA Specification.

MCH Pin # and Signal Connector 1	AMC Pin # and Signal
MCH1-163 TxFA-1+	AMC1-14 Rx0+
MCH1-162 TxFA-1-	AMC1-15 Rx0-
MCH1-160 TxFA-1+	AMC1-11 Tx0+
MCH1-159 TxFA-1-	AMC1-12 Tx0-
MCH1-157 TxFA-2+	AMC2-14 Rx0+
MCH1-156 TxFA-2-	AMC2-15 Rx0-
MCH1-154 RxFA-2+	AMC2-11 Tx0+
MCH1-153 RxFA-2-	AMC2-12 Tx0-
MCH1-20 TxFA-3+	AMC3-14 Rx0+
MCH1-21 TxFA-3-	AMC3-15 Rx0-
MCH1-23 RxFA-3+	AMC3-11 Tx0+
MCH1-24 RxFA-3-	AMC3-12 Tx0-
MCH1-151 TxFA-4+	AMC4-14 Rx0+
MCH1-150 TxFA-4-	AMC4-15 Rx0-
MCH1-148 RxFA-4+	AMC4-11 Tx0+
MCH1-147 RxFA-4-	AMC4-12 Tx0-
MCH1-29 TxFA-5+	AMC5-14 Rx0+
MCH1-30 TxFA-5-	AMC5-15 Rx0-
MCH1-32 RxFA-5+	AMC5-11 Tx0+
MCH1-33 RxFA-5-	AMC5-12 Tx0-
MCH1-145 TxFA-6+	AMC6-14 Rx0+
MCH1-144 TxFA-6-	AMC6-14 Rx0-
MCH1-142 RxFA-6+	AMC6-11 Tx0+
MCH1-141 RxFA-6-	AMC6-12 Tx0-
MCH1-35 TxFA-7+	AMC7-14 Rx0+
MCH1-36 TxFA-7-	AMC7-15 Rx0-
MCH1-38 RxFA-7+	AMC7-11 Tx0+
MCH1-39 RxFA-7-	AMC7-12 Tx0-
MCH1-139 TxFA-8+	AMC7-14 Rx0+
MCH1-138 TxFA-8-	AMC7-15 Rx0-
MCH1-136 TxFA-8+	AMC7-11 Tx0+
MCH1-135 TxFA-8-	AMC7-12 Tx0-
MCH1-44 TxFA-9+	AMC7-14 Rx0+
MCH1-45 TxFA-9-	AMC7-15 Rx0-
MCH1-47 RxFA9+	AMC7-11 Tx0+
MCH1-48 RxFA-9-	AMC7-12 Tx0-
MCH1-50 TxFA-10+	AMC7-14 Rx0+
MCH1-51 TxFA-10-	AMC7-15 Rx0-
MCH1-53 RxFA-10+	AMC7-11 Tx0+
MCH1-54 RxFA-10-	AMC7-12 Tx0-
MCH2-163 TxFA-1+	AMC1-14 Rx0+
MCH2-162 TxFA-1-	AMC1-15 Rx0-
MCH2-160 RxFA-1+	AMC1-11 Tx0+
MCH2-159 RxFA-1-	AMC1-12 Tx0-
MCH2-157 TxFA-2+	AMC2-14 Rx0+
MCH2-156 TxFA-2-	AMC2-15 Rx0-
MCH2-154 RxFA-2+	AMC2-11 Tx0+
MCH2-153 RxFA-2-	AMC2-12 Tx0-
MCH2-20 TxFA-3+	AMC3-14 Rx0+
MCH2-21 TxFA-3-	AMC3-15 Rx0-

MICROTCA USER MANUAL-DUAL STAR BACKPLANE

FABRIC INTERFACE (CONTINUED)

MCH Fabric [A] is routed to AMC Port [0] on each slot. See below for a netlist. Reference section 6.2 in the MicroTCA Specification.

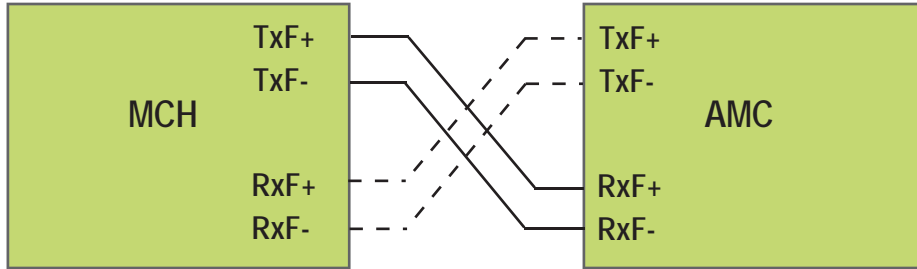
MCH Pin # and Signal Connector 1	AMC Pin # and Signal
MCH2-23 RxFA-3+	AMC3-11 Tx0+
MCH2-24 RxFA-3-	AMC3-12 Tx0-
MCH2-151 TxFA-4+	AMC4-14 Rx0+
MCH2-150 TxFA-4-	AMC4-15 Rx0-
MCH2-148 RxFA-4+	AMC4-11 Tx0+
MCH2-147 RxFA-4-	AMC4-12 Tx0-
MCH2-29 TxFA-5+	AMC5-14 Rx0+
MCH2-30 TxFA-5-	AMC5-15 Rx0-
MCH2-32 RxFA-5+	AMC5-11 Tx0+
MCH2-33 RxFA-5-	AMC5-11 Tx0-
MCH2-145 TxFA-6+	AMC6-14 Rx0+
MCH2-144 TxFA-6-	AMC6-15 Rx0-
MCH2-142 RxFA-6+	AMC6-11 Tx0+
MCH2-141 RxFA-6-	AMC6-12 Tx0-
MCH2-35 TxFA-7+	AMC7-14 Rx0+
MCH2-36 TxFA-7-	AMC7-15 Rx0-
MCH2-38 RxFA-7+	AMC7-11 Tx0+
MCH2-39 RxFA-7-	AMC7-12 Tx0-
MCH2-139 TxFA-8+	AMC7-14 Rx0+
MCH2-138 TxFA-8-	AMC7-15 Rx0-
MCH2-136 RxFA-8+	AMC7-11 Tx0+
MCH2-135 RxFA-8-	AMC7-12 Tx0-
MCH2-44 TxFA-9+	AMC7-14 Rx0+
MCH2-45 TxFA-9-	AMC7-15 Rx0-
MCH2-47 RxFA-9+	AMC7-11 Tx0+
MCH2-48 RxFA-9-	AMC7-12 Tx0-
MCH2-50 TxFA-10+	AMC7-14 Rx0+
MCH2-51 TxFA-10-	AMC7-15 Rx0+
MCH2-53 RxFA-10+	AMC7-11 Tx0+
MCH2-54 RxFA-10-	AMC7-12 Tx0-

MCH Fabric [D:G] (D,E,F and G) is routed to AMC Port [4:7] (4,5,6 and 7) on each slot. Follow the example of Fabric A above.

MICROTCA USER MANUAL-DUAL STAR BACKPLANE

FABRIC CROSS-OVER ROUTING

The transmit and receive pairs shall be cross-over routed, see the figure below.



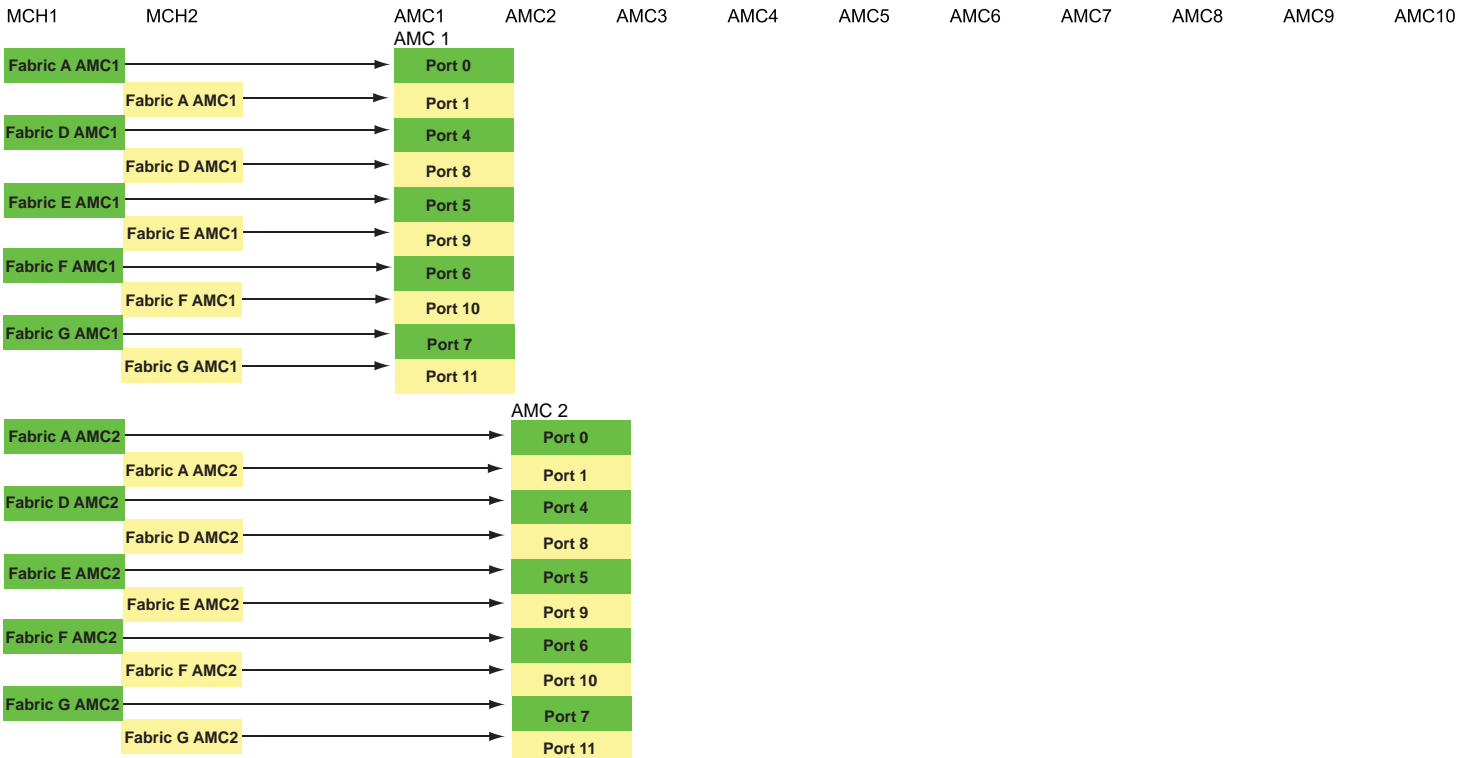
The differential impedance of the serial links for the fabric interface shall be 100 Ohms ± 10%. Signal lengths within the differential pair should be matched to better than 3.4 ps (0.5mm in FR4 at e(r)=4.0). The transmit and receive pairs within a channel should each have a matched delay of better than 17ps (2.54mm in FR4 at e(r)=4.0). Transmit and receive pairs may be unmatched to each other.

The JTAG interface is not implemented.

Notes:
The pin numbers and signal names were typed in manually and there may be mistakes. If there is a discrepancy, the MicroTCA and AMC Specifications take precedence.

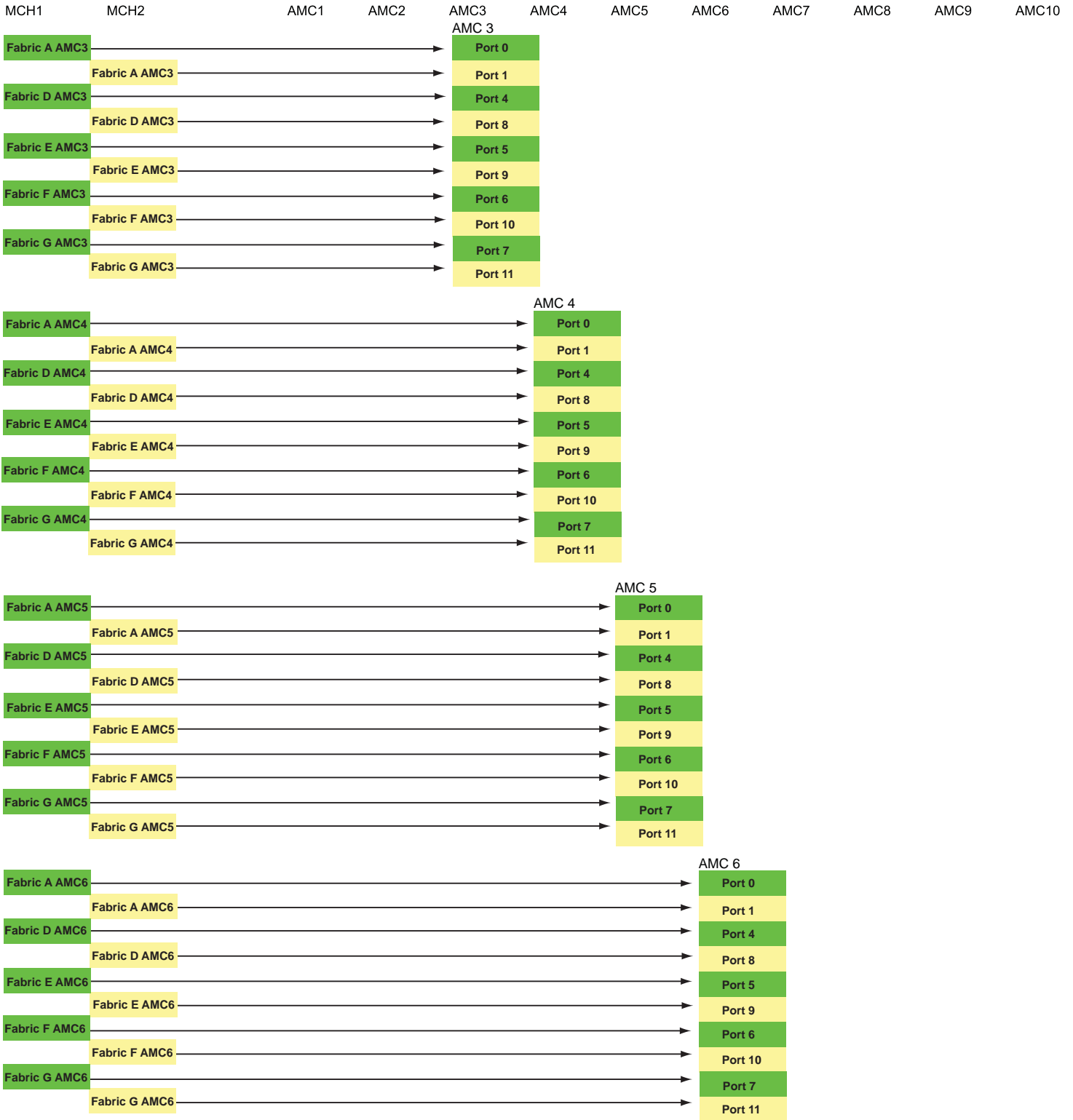
Single-ended signal impedance shall be 65 Ohm +/- 10%.

LANE MAPPING



MICROTCA USER MANUAL-DUAL STAR BACKPLANE

LANE MAPPING



MICROTCA USER MANUAL-DUAL STAR BACKPLANE

LANE MAPPING

